R.M.K. ENGINEERING COLLEGE

RSM NAGAR, KAVARAIPETTAI – 601 206

(An Autonomous Institution, Affiliated to Anna University, Chennai)

M.E.APPLIED ELECTRONICS

REGULATIONS – 2020

CHOICE BASED CREDIT SYSTEM

Curriculum and Syllabus

Master of Engineering

Applied Electronics

Vision and Mission of the Department

Vision:

- To be one of the most sought after Centers of Excellence in the field of Electronics and Communication Engineering by providing High Quality Education.
- To mould the students to compete Internationally and to become Excellent Researchers and innovators who can provide solution to societal issues

Mission:

- To provide the needed resources and infrastructure and to establish a Conducive Ambience for the Teaching-Learning and Research Processes and to meet with the technological developments.
- To create High Quality Professionals and Entrepreneurs in the field of Electronics and Communication Engineering with the right attitude to serve the society with ethical values.
- To Modernize the Laboratories on par with industry standards and to collaborate with them to improve the skill set of the students for providing Innovative Solutions to the Industry.
- To provide a good ambience which encourages the students to Pursue Higher Education.

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PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

PEO1:	Graduates will develop the ability to Identify, Formulate and Solve Challenging Problems in the field of Electronics and Communication Engineering.
PEO 2:	Graduates will acquire the Professional Skills that make them ready for Immediate Employment or to Pursue Higher Studies in the related disciplines.
PEO 3:	Graduates will be molded with a Strong Educational Foundation that Prepares them for Leadership Roles
PEO 4:	Graduates will show the understanding of Impact of Engineering Solutions in the Society and also will be aware of Contemporary Issues
PEO 5:	Graduates will develop Confidence to Communicate their Ideas effectively to Industry and Society

Program Specific Objectives(PSOs):

PSO1:	Apply the principles of Semiconductor Devices, Digital Systems, Microprocessor and Signal Processing in the fields of Consumer Electronics, Medical, Defence and Spacecraft Electronics industry.
PSO 2:	Design a variety of Computer-based Components and Systems for applications including Communications, Networking and Control Systems.
PSO 3:	Develop Indigenous Components and methods for producing High Quality, Compact, Energy Efficient and Eco-Friendly consumer goods at an affordable price.

Program Outcomes (POs):

Upon completion of the Programme, Graduates will

a) **Engineering Knowledge:** Apply the knowledge of mathematics, science, engineering fundamentals and an engineering specialization to the solution of complex engineering problems.

b) **Problem analysis :** Identify, formulate, review research literature, and analyse complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences

c) **Design / development of solutions:** Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.

d) **Conduct investigations of complex problems:** Use research-based knowledge and research methods, including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

e) **Modern tool usage :** Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modelling to complex engineering activities with an understanding of the limitations
f) **The Engineer and Society :** Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice
g) **Environment and sustainability:** Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainable development.
h) **Ethics :** Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice
i) **Individual and team work :** Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings
j) **Communication:** Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
k) **Project Management and finance :** Demonstrate knowledge and understanding of the engineering and management principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments
l) **Life-long learning:** Recognize the need for, and have the preparation and ability to engage in independent and lifelong learning in the broadest context of technological change.

Mapping of Programme Educational Objectives with Programme Outcomes:

The correlation between the defined POs and the PEOs is given in Table

Table 2: Correlation between the defined POs and the PEOs

PEOs	Graduate Attributes/POs											
	A	b	c	d	e	f	g	h	i	j	k	l
PEO1	3	3	3	3	3	3	2	3	3	3	3	3
PEO2	3	3	3	3	2	2	2	3	3	3	3	3
PEO3	3	3	3	2	2	2	2	3	2	3	2	2
PEO4	2	2	2	2	2	2	3	3	3	2	3	2
PEO5	3	3	3	3	3	2	3	2	2	3	2	3

Mapping of Programme Specific Outcomes (PSOs) and the Program Outcomes (POs):

The correlation between the defined POs and the PSOs is given in Table

PSOs	Graduate Attributes/POs											
	A	b	c	d	e	f	g	h	i	j	k	l
PSO1	3	3	3	3	3	2	2	2	2	2	3	3
PSO2	3	3	3	3	3	1	1	1	2	2	1	2
PSO3	3	3	3	3	1	2	2	1	2	2	2	2

M.E. APPLIED ELECTRONICS
SEMESTER COURSE WISE PO MAPPING

MAPPING OF COURSE OUTCOMES WITH PROGRAMME OUTCOMES:

A broad relation between the Course Outcomes and Programme Outcomes is given in the following table

	Sem	COURSE OUTCOMES	PROGRAMME OUTCOMES											
		Course Name	a	b	c	d	e	f	g	h	i	j	k	l
I YEAR	I	Applied Mathematics for Electronics Engineers	3	3	2	1	0	0	0	2	2	3	0	3
		Advanced Digital System Design	3	2	2	2	1	0	0	3	2	3	0	2
		Advanced Digital Signal Processing	3	2	2	2	1	0	0	3	2	3	0	2
		Embedded System Design	3	2	2	2	2	0	0	3	2	3	0	2
		Sensors, Actuators and System Interface	3	2	2	1	0	0	0	3	2	3	0	2
		PROFESSIONAL ELECTIVE I												
		RF Test and Measurement	3	3	3	3	3	1	1	1	1	1	2	2
		DSP Processor Architecture and Programming	3	2	2	2	2	0	0	3	2	3	0	2
		Computer Architecture and Parallel Processing	3	2	2	1	0	0	0	3	2	3	0	2
		Electromagnetic Interference and Compatibility	3	2	2	1	0	1	0	3	2	3	0	2
		PRACTICALS												
		Electronic System Design Laboratory	3	2	2	2	2	0	0	3	3	3	0	2
		Technical Seminar	3	3	0	2	3	0	0	3	2	2	2	2
	II	Digital CMOS VLSI Design	3	2	2	1	1	0	0	0	1	1	0	1
		Hardware – Software Co-design	3	2	2	2	0	0	0	3	2	3	0	2
		IOT System Design and Security	3	3	2	2	0	0	0	2	1	2	0	2
		PROFESSIONAL ELECTIVE II												
		Reconfigurable VLSI Architectures	3	2	2	2	2	2	0	0	1	1	0	1
		Nano Electronics and Technology	3	2	2	1	2	2	1	2	1	1	1	1
		Programming Languages for Embedded Software	3	3	3	2	2	0	0	2	2	2	0	2
		Advanced Microprocessors and Microcontrollers	3	3	3	2	2	0	0	3	3	3	0	2
		PROFESSIONAL ELECTIVE III												
		Wireless Adhoc and Sensor Networks	3	2	1	0	0	0	0	3	2	3	0	2
		High Performance Networks	3	2	1	0	0	0	0	3	2	3	0	2
		Cryptography and Network Security	3	3	3	3	2	3	1	1	3	2	1	2
		Multimedia Compression Techniques	3	2	3	3	1	0	0	0	1	0	0	1
		PROFESSIONAL ELECTIVE IV												
		MEMS Based Devices	3	2	2	1	1	0	0	3	2	3	0	2
		Smart Antennas	3	2	3	3	3	1	2	1	1	1	2	2
		RF IC Design	3	3	3	2	2	0	0	1	0	0	0	1
		Microwave Integrated Circuits	3	2	3	3	3	1	2	1	1	1	2	2
		PRACTICALS												
		Analog and Digital CMOS VLSI Design Laboratory	3	2	2	2	2	1	1	3	2	3	1	2
		Mini Project and Term Paper Writing	3	2	2	2	2	2	2	1	2	2	1	2

	Sem	COURSE OUTCOMES	PROGRAMME OUTCOMES										
		Course Name	**a**	**b**	**c**	**d**	**e**	**f**	**g**	**h**	**i**	**j**	**k**	**l**
II YEAR	**III**	Advanced Digital Image Processing	3	2	2	2	1	0	0	3	2	3	0	2
		PROFESSIONAL ELECTIVE V												
		Pattern Recognition and Machine learning	3	3	2	3	3	3	0	2	3	3	3	2
		Data Converters	3	3	3	2	2	0	0	1	0	0	0	1
		Solid State Device Modeling and Simulation	3	2	2	1	0	0	0	3	2	3	0	2
		Speech and Audio Signal Processing	3	2	2	1	1	0	0	3	2	3	0	2
		PROFESSIONAL ELECTIVE VI												
		Physical Design of VLSI Circuit	3	2	2	1	0	0	0	3	2	3	0	2
		Robotics and Intelligent Systems	3	2	2	2	1	0	0	3	2	3	0	1
		System on Chip Design	3	2	2	1	1	0	0	3	2	3	0	2
		Foundations of Artificial Intelligence and Data Science	3	2	2	2	1	0	0	3	2	3	0	2
		PRACTICALS												
		Project Work Phase I	3	3	3	3	3	2	2	3	3	3	3	3
	IV	Project Work Phase-II	3	3	3	3	3	2	2	3	3	3	3	3

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CURRICULA AND SYLLABI

Semester I

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	20MA101	Applied Mathematics for Electronics Engineers	FC	4	4	0	0	4
2	20AE101	Advanced Digital System Design	PC	3	3	0	0	3
3	20AE102	Advanced Digital Signal Processing	PC	5	3	2	0	4
4	20AE103	Embedded System Design	PC	3	3	0	0	3
5	20AE104	Sensors, Actuators and Interface Electronics	PC	3	3	0	0	3
6		Professional Elective I	PE	3	3	0	0	3
PRACTICALS								
7	20AE111	Electronic System Design Laboratory	PC	4	0	0	4	2
8	20AE112	Technical Seminar	EEC	2	0	0	2	1
TOTAL				**27**	**19**	**2**	**6**	**23**

Semester II

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	20AE201	Digital CMOS VLSI Design	PC	3	3	0	0	3
2	20AE202	Hardware – Software Co-design	PC	3	3	0	0	3
3	20AE203	IOT System Design and Security	PC	3	3	0	0	3
4		Professional Elective II	PE	3	3	0	0	3
5		Professional Elective III	PE	3	3	0	0	3
6		Professional Elective IV	PE	3	3	0	0	3
PRACTICALS								
7	20AE211	Analog and Digital CMOS VLSI Design Laboratory	PC	4	0	0	4	2
8	20AE212	Mini Project and Term Paper Writing	EEC	2	0	0	2	2
TOTAL				**24**	**18**	**0**	**6**	**22**

Semester III

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
THEORY								
1	20AE301	Advanced Digital Image Processing	PC	3	3	0	0	3
2		Professional Elective V	PE	3	3	0	0	3
3		Professional Elective VI	PE	3	3	0	0	3
PRACTICALS								
4	20AE311	Project Work Phase I	EEC	12	0	0	12	6
TOTAL				**21**	**9**	**0**	**12**	**15**

Semester IV

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
PRACTICALS								
6	20AE411	Project Work Phase-II	EEC	24	0	0	24	12
TOTAL				**24**	**0**	**0**	**24**	**12**

TOTAL NO. OF CREDITS: 72

CATEGORIZATION OF COURSES

FOUNDATION COURSES (FC)

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20MA101	Applied Mathematics for Electronics Engineers	FC	4	4	0	0	4

PROFESSIONAL CORE (PC)

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20AE101	Advanced Digital System Design	PC	3	3	0	0	3
2	20AE102	Advanced Digital Signal Processing	PC	5	3	2	0	4
3	20AE103	Embedded System Design	PC	3	3	0	0	3
4	20AE104	Sensors, Actuators and Interface Electronics	PC	3	3	0	0	3
5	20AE111	Electronic System Design Laboratory	PC	4	0	0	4	2
6	20AE201	Digital CMOS VLSI Design	PC	3	3	0	0	3
7	20AE202	Hardware – Software Co-design	PC	3	3	0	0	3
8	20AE203	IOT System Design and Security	PC	3	3	0	0	3
9	20AE211	Analog and Digital CMOS VLSI Design Laboratory	PC	4	0	0	4	2
10	20AE301	Advanced Digital Image Processing	PC	3	3	0	0	3

EMPLOYABILITY ENHANCEMENT COURSE (EEC)

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20AE112	Technical Seminar	EEC	2	0	0	2	1
2	20AE212	Mini Project and Term Paper Writing	EEC	2	0	0	2	1
3	20AE311	Project Work Phase-I	EEC	12	0	0	12	6
4	20AE411	Project Work Phase-II	EEC	24	0	0	24	12

PROFESSIONAL ELECTIVES (PE)

SEMESTER I
ELECTIVE I

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20AE121	RF Test and Measurement	PE	3	3	0	0	3
2	20AE122	DSP Processor Architecture and Programming	PE	3	3	0	0	3
3	20AE123	Computer Architecture and Parallel Processing	PE	3	3	0	0	3
4	20AE124	Electromagnetic Interference and Compatibility	PE	3	3	0	0	3

SEMESTER II
ELECTIVE – II

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20AE221	Reconfigurable VLSI Architectures	PE	3	3	0	0	3
2	20AE222	Nano Electronics and Technology	PE	3	3	0	0	3
3	20AE223	Programming Languages for Embedded Software	PE	3	3	0	0	3
4	20AE224	Advanced Microprocessors and Microcontrollers	PE	3	3	0	0	3

ELECTIVE – III

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20AE225	Wireless Adhoc and Sensor Networks	PE	3	3	0	0	3
2	20AE226	High Performance Networks	PE	3	3	0	0	3
3	20AE227	Cryptography and Network Security	PE	3	3	0	0	3
4	20AE228	Multimedia Compression Techniques	PE	3	3	0	0	3

ELECTIVE – IV

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20AE229	MEMS Based Devices	PE	3	3	0	0	3
2	20AE230	Smart Antennas	PE	3	3	0	0	3
3	20AE231	RF IC Design	PE	3	3	0	0	3
4	20AE232	Microwave Integrated Circuits	PE	3	3	0	0	3

SEMESTER III

ELECTIVE – V

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20AE321	Pattern Recognition and Machine learning	PE	3	3	0	0	3
2	20AE322	Data Converters	PE	3	3	0	0	3
3	20AE323	Solid State Device Modeling and Simulation	PE	3	3	0	0	3
4	20AE324	Speech and Audio Signal Processing	PE	3	3	0	0	3

ELECTIVE – VI

Sl. No.	Course Code	Course Title	Category	Contact Periods	L	T	P	C
1	20AE325	Physical Design of VLSI Circuit	PE	3	3	0	0	3
2	20AE326	Robotics and Intelligent Systems	PE	3	3	0	0	3
3	20AE327	System on Chip Design	PE	3	3	0	0	3
4	20AE328	Foundations of Artificial Intelligence and Data Science	PE	3	3	0	0	3

DISTRIBUTION OF CREDITS

Sl. No.	Category	Credits as per Semester				Total Credits	Percentage
		I	II	III	IV		
1	FC	4	-	-	-	4	5.55
2	PC	15	11	3	-	29	40.28
3	EEC	1	2	6	12	21	29.17
4	PE	3	9	6	-	18	25

COMPARISON TABLE- DISTRIBUTION OF CREDITS

Sl. No.	Statutory Bodies	Credits as per Semester				Total Credits
		I	II	III	IV	
1	AICTE	18	18	16	16	**68**
2	Anna University- Department	19	21	18	12	**70**
3	Anna University-Affiliated Colleges	22	21	15	12	**70**
4	RMKEC	23	22	15	12	**72**

COURSE CODE	COURSE TITLE	L	T	P	C
20MA101	APPLIED MATHEMATICS FOR ELECTRONICS ENGINEERS	4	0	0	4

OBJECTIVES:

- Impart the knowledge of Fuzzy set and Fuzzy logic.
- Introduce the idea of matrix decomposition.
- Implement the fundamental concept of probability.
- Acquaint the students with the concepts of dynamic programming.
- Develop an understanding on the concepts of queuing theory.

UNIT I FUZZY LOGIC **12**

Classical logic – Multivalued logics – Fuzzy propositions – Fuzzy quantifiers.

UNIT II MATRIX THEORY **12**

Cholesky decomposition – Generalized Eigenvectors – Canonical basis – QR factorization – Least squares method – Singular value decomposition.

UNIT III PROBABILITY AND RANDOM VARIABLES **12**

Probability – Axioms of probability – Conditional probability – Baye's Theorem – Random variables – Probability function – Moments – moment generating function.

UNIT IV DYNAMIC PROGRAMMING **12**

Dynamic programming – Principle of optimality – Forward and backward recursion – Applications of dynamic programming – Problem of Dimensionality.

UNIT V QUEUING MODELS **12**

Poisson Process – Markovian queues – Single and Multi-server Models – Little's formula – Machine Interference Model – Steady State analysis - Self-service queue.

TOTAL PERIODS: 60

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Apply the concept of fuzzy logic in real life problem.
CO2: Execute the matrix decomposition in engineering problems.
CO3: Make use of probability concepts in problems of uncertainty
CO4: Use dynamic programming for optimization.
CO5: Analyze and apply the various queuing models.
CO6: Solve problems in engineering domain related to random variables.

REFERENCE BOOKS:

1. R. Bronson, Matrix Operations, Schaum's Outline Series, First Edition, McGraw Hill, 2011.
2. George, J. Klir and B. Yuan, Fuzzy sets and Fuzzy logic, Theory and Applications, Prentice Hall of India Private Limited, First Edition, 1997.
3. D. Gross, J. F. Shortle, J. M. Thompson, and C. M. Harris, Fundamentals of Queuing Theory, Fourth Edition, and John Wiley, 2014.
4. R. A. Johnson, I. Miller and J. Freund, Miller and Freund's Probability and Statistics for Engineers, Pearson Education, Asia, Eighth Edition, 2015.
5. H.A. Taha, Operations Research: An Introduction, Ninth Edition, Pearson Education, Asia,

New Delhi, 2016.
6. John F. Shortle, James M. Thompson, Donald Gross, Carl M. Harris, Fundamentals of Queuing Theory, 5th Edition Wiley, 2018.

NPEL: https://nptel.ac.in/courses/111/107/111107119/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE101	ADVANCED DIGITAL SYSTEM DESIGN	3	0	0	3

OBJECTIVES:

- To introduce methods to analyze and design synchronous and asynchronous sequential circuits.
- To introduce the architectures of programmable devices.
- To introduce design and implementation of digital circuits using programming tools.
- To design and implement digital circuits using HDL.
- To introduce the fault testing procedure for combinational circuits and PLA circuits.

UNIT I SEQUENTIAL CIRCUIT DESIGN 9

Analysis of clocked synchronous sequential circuits and modeling - State diagram, state table, state table assignment and reduction - Design of synchronous sequential circuits - Design of iterative circuits - ASM chart and realization using ASM

UNIT II ASYNCHRONOUS SEQUENTIAL CIRCUIT DESIGN 9

Analysis of asynchronous sequential circuit – Flow table reduction – Races - state assignment - Transition table and problems in transition table - design of asynchronous sequential circuit -Static, dynamic and essential hazards – Data synchronizers – Mixed operating mode asynchronous circuits – designing vending machine controller.

UNIT III FAULT DIAGNOSIS AND TESTABILITY ALGORITHMS 9

Fault table method - Path sensitization method – Boolean difference method - D algorithm - Tolerance techniques – The compact algorithm – Fault in PLA – Test generation - DFT schemes – Built in self-test

UNIT IV SYSTEM DESIGN USING VERILOG 9

Hardware Modeling with Verilog HDL – Logic System, Data Types and Operators for Modeling in Verilog HDL - Behavioural Descriptions in Verilog HDL – HDL Based Synthesis – Synthesis of Finite State Machines– structural modeling – compilation and simulation of Verilog code – Test bench - Realization of combinational and sequential circuits using Verilog – Registers – Counters – Sequential machine – Serial adder – Multiplier- Divider

UNIT V PROGRAMMABLE DEVICES 9

Programming logic device families – FPGA – Xilinx FPGA - Xilinx 4000, CPLD, SoC FPGAs, Xilinx Zync 7000 series, Altera cyclone 2

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Design and analyze synchronous and asynchronous sequential circuits.

CO2: Design asynchronous hazard free sequential circuits.

CO3: Apply appropriate testing algorithms to detect the fault.

CO4: Analyze combinational, sequential circuits using Verilog.

CO5: Design and Analyse sequential circuits in high end FPGAs with SoC architecture.

CO6: Learn the benefits and drawbacks of the various design methods for solving a problem.

REFERENCE BOOKS:

1. Charles H. Roth Jr, Fundamentals of Logic Design, Thomson Learning, Seventh Edition, 2014.
2. Nripendra N Biswas, Logic Design Theory, Prentice Hall of India, 2010.
3. Parag K. Lala, Fault Tolerant and Fault Testable Hardware Design, B S Publications, 2002.
4. Parag K. Lala, Digital System Design using PLD, B S Publications, 2003.
5. Louise H. Crockett, Ross A. Elliot, Martin A. Enderwitz, Robert W. Stewart, The Zynq Book - Embedded Processing with the ARM Cortex-A9 on the Xilinx Zynq-7000 All Programmable SoC, Strathclyde Academic Media, 2014.
6. Palnitkar S, Verilog HDL – A Guide to Digital Design and Synthesis, Pearson, 2003.

NPEL: https://nptel.ac.in/courses/108/105/108105113/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE102	ADVANCED DIGITAL SIGNAL PROCESSING	3	2	0	4

OBJECTIVES:

- To comprehends mathematical description and modelling of discrete time random signals
- To conversant with important theorems and random signal processing algorithms
- To learns relevant figures of merit such as power, energy, bias and consistency.
- To analyze multirate DSP systems
- To familiar with estimation, prediction, filtering, and techniques.

UNIT I DISCRETE RANDOM SIGNAL PROCESSING **12**

Discrete random processes – Ensemble averages – Wide sense stationary process – Properties - Ergodic process – Sample mean & variance - Auto-correlation and Auto-correlation matrices-Properties – White noise process – Weiner Khitchine relation - Power spectral density – Filtering random process – Spectral Factorization Theorem – Special types of Random Processes – ARMA, ARMA Processes – Yule-Walker equations.

UNIT II SPECTRUM ESTIMATION **12**

Bias and Consistency of estimators - Non-Parametric methods – Periodogram – Modified Periodogram – Barlett's method – Welch's method – Blackman-Tukey method – Parametric methods – ARMA and ARMA spectrum estimation - Performance analysis of estimators

UNIT III SIGNAL MODELING AND OPTIMUM FILTERS **12**

Introduction- Least square method – Pade approximation – Prony's method – Levinson Recursion – Lattice filter - FIR Wiener filter – Filtering – Linear Prediction – Non-Causal and Causal IIR Weiner Filter –- Mean square error – Discrete Kalman filter.

UNIT IV ADAPTIVE FILTERS **12**

FIR Adaptive filters - Newton's steepest descent method – Widrow Hoff LMS Adaptive algorithm – Convergence – Normalized LMS – Applications – Noise cancellation - channel equalization – echo canceller – Adaptive Recursive Filters - RLS adaptive algorithm – Exponentially weighted RLS-sliding window RLS.

UNIT V MULTIRATE SIGNAL PROCESSING **12**

Decimation - Interpolation – Sampling Rate conversion by a rational factor I/D – Multistage implementation of sampling rate conversion – Polyphase filter structures – Applications of multirate signal processing

TOTAL PERIODS: 60

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Formulate time domain and frequency domain description of Wide Sense Stationary process in terms of matrix algebra and relate to linear algebra concepts.

CO2: State W-K theorem, spectral factorization theorem, spectrum estimation, bias and consistency of estimators

CO3: Study the Wiener filtering, LMS algorithms, Levinson recursion algorithm, applications of adaptive filters

CO4: Analyze the Decimation, interpolation, Sampling rate conversion, Applications of multirate signal processing

CO5: Describe the statistical properties of the conventional spectral estimators.

CO6: Apply the algorithms for wide area of recent applications.

REFERENCE BOOKS:

1. John G. Proakis, Dimitris G. Manolakis, Digital Signal Processing: Principles, Algorithms and Applications, Fifth Edition Pearson, New Delhi, 2021.
2. Monson H. Hayes, Statistical Digital Signal Processing and Modeling, John Wiley and Sons Inc., New York, 2006.
3. P. P. Vaidyanathan, Multirate Systems and Filter Banks, Prentice Hall, 1992.
4. S. Kay, Modern spectrum Estimation theory and application, Prentice Hall, Englehood Cliffs, NJ1988.
5. Simon Haykin, Adaptive Filter Theory, Prentice Hall, Englehood Cliffs, NJ1986
6. Sophoncles J. Orfanidis, Optimum Signal Processing, McGraw-Hill, 2000.

NPTEL: https://nptel.ac.in/courses/117/105/117105135/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE103	EMBEDDED SYSTEM DESIGN	3	0	0	3

OBJECTIVES:

- To expose the students to the fundamentals of embedded system design
- To enable the students to understand and use embedded computing platform
- To introduce networking principles in embedded devices.
- To learn real time characteristics in embedded system design
- To explore system design techniques.

UNIT I EMBEDDED PROCESSORS **9**

Embedded Computers, Characteristics of Embedded Computing Applications, Challenges in Embedded Computing system design, Embedded system design process- Requirements, Specification, Architectural Design, Designing Hardware and Software Components, System Integration, Formalism for System Design- Structural Description, Behavioural Description, Design Example: Model Train Controller, ARM processor- processor and memory organization

UNIT II EMBEDDED COMPUTING PLATFORM **9**

Data operations, Flow of Control, SHARC processor- Memory organization, Data operations, Flow of Control, parallelism with instructions, CPU Bus configuration, ARM Bus, SHARC Bus, Memory devices, Input/output devices, Component interfacing, designing with microprocessor development and debugging, Design Example : Alarm Clock

UNIT III NETWORKS **9**

Distributed Embedded Architecture- Hardware and Software Architectures, Networks for embedded systems- I^2C, CAN Bus, SHARC link supports, Ethernet, Myrinet, Internet, Network- Based design- Communication Analysis, system performance Analysis, Hardware platform design, Allocation and scheduling, Design Example: Elevator Controller.

UNIT IV REAL-TIME CHARACTERISTICS **9**

Clock driven Approach, weighted Round Robin Approach, Priority driven Approach, Dynamic Versus Static systems, effective release times and deadlines, Optimality of the Earliest deadline first (EDF) algorithm, challenges in validating timing constraints in priority driven systems, Off- line Versus On-line scheduling

UNIT V SYSTEM DESIGN TECHNIQUES **9**

Design Methodologies, Requirement Analysis, Specification, System Analysis and Architecture Design, Quality Assurance, Design Example: Telephone PBX- System Architecture, Ink jet printer- Hardware Design and Software Design, Personal Digital Assistants, Set-top Boxes.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Explore fundamentals of embedded system design.

CO2: Interpret and use embedded computing platform.

CO3: Apply networking principles in embedded devices.

CO4: Gain insight on the characteristics in embedded system design.

CO5: Select and design suitable embedded systems for real world applications.

CO6: Analyze to understand different concepts of a RTOS, sensors, memory interface, and communication interface.

REFERENCE BOOKS:

1. Wayne Wolf, Computers as Components: Principles of Embedded Computing System Design, Morgan Kaufman Publishers, Third Edition, 2013.
2. Jane.W.S. Liu, Real-Time systems, Pearson Education Asia, 2001.
3. C. M. Krishna and K. G. Shin, Real-Time Systems, Third Edition, McGraw-Hill, 2010.
4. Frank Vahid and Tony Givargis, Embedded System Design: A Unified Hardware/Software Introduction, John Wiley & Sons, 2002.
5. Jiacun Wang, Real-Time Embedded Systems, Wiley, 2017.
6. Uwe Meyer-Baese, Embedded Microprocessor System Design using FPGAs, Springer, 2021.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE104	SENSORS, ACTUATORS AND INTERFACE ELECTRONICS	3	0	0	3

OBJECTIVES:

- To understand the static and dynamic characteristics of measurement systems
- To introduce the various types of sensors
- To introduce different types of actuators and their usage
- To compare state-of-the-art digital and semiconductor sensors
- To study interfacing and communication system of sensors

UNIT I INTRODUCTION TO MEASUREMENT SYSTEMS 9

Introduction to measurement systems: general concepts and terminology – measurement systems, sensor classification – general input-output configuration, methods of correction –Performance characteristics**:** static characteristics and dynamic characteristics of measurement systems: zero-order – first-order – and second-order measurement systems and response

UNIT II RESISTIVE AND REACTIVE SENSORS 9

Resistive sensors: potentiometers, strain gauges – resistive temperature detectors(RTD) – Thermistors – magneto resistors – light-dependent resistors – Signal conditioning for resistive sensors: Wheatstone bridge – sensor bridge calibration and compensation – Reactance variation and electromagnetic sensors: capacitive sensors – differential – inductive sensors –Linear Variable Differential Transformers (LVDT) – application and signal conditioning of LVDT – magneto elastic sensors – hall effect sensors

UNIT III SELF-GENERATING SENSORS 9

Self-generating sensors: thermoelectric sensors – piezoelectric sensors, pyroelectric sensors – photovoltaic sensors – electrochemical sensors – Signal conditioning for self-generating sensors: chopper and low-drift amplifiers – electrometer amplifiers – charge amplifiers – noise in charge amplifiers

UNIT IV ACTUATORS DRIVE CHARACTERISTICS AND APPLICATIONS 9

Relays, Solenoid drive – Stepper Motors – Voice-Coil actuators – Hydraulic actuators – Variable transformers: synchros – resolvers – Inductosyn – resolver-to-digital and digital-to-resolver converter

UNIT V DIGITAL AND INTELLIGENT SENSORS 9

Digital sensors: position encoders, Resonant sensors– quartz digital thermometer – SAW sensors – vibrating wire strain gauges – vibrating cylinder sensors – digital flow meters - photodiodes and phototransistors. Sensors based on MOSFET transistors – CCD imaging sensors – ultrasonic sensors – fiber-optic sensors – Bio Sensors – Direct Sensor – Microcontroller Interfacing – Communication system for sensors – Intelligent sensors

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Compare different types of sensors and actuators

CO2: Evaluate digital sensors and semiconductor device sensors

CO3: Analyse the various self-generating sensors

CO4: Interface sensors for various applications

CO5: Compare the properties of analog and digital sensors.

CO6: Create analytical design and development solutions for sensors and actuators

REFERENCE BOOKS:

1. Doeblin E.O, Measurement System: Applications and Design, McGraw Hill publications, Second Edition, 2000.
2. Ramon PallásAreny, John G. Webster, Sensors and Signal conditioning, John Wiley and Sons, Second Edition, 2000.
3. Andrzej M. Pawlak Sensors and Actuators in Mechatronics Design and Applications, CRC Press, 2006.
4. Patranabis D, Sensors and Transducers, Tata McGraw Hill, Seventh Edition, 2003.
5. Kevin James, PC Interfacing and Data acquisition, Elsevier, 2011.
6. Nathan Ida, Sensors, Actuators, and Their Interfaces: A Multidisciplinary Introduction, Control, Robotics and Sensors, 2020.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE111	ELECTRONIC SYSTEM DESIGN LABORATORY	0	0	4	2

OBJECTIVES:

- To study of different interfaces.
- To learn about Circuit Level Design, Post Layout and Simulation to analyze Frequency Response, Noise and Stability for analog circuits.
- To know use of Verilog and VHDL in modelling combinational and sequential digital systems

- To learn the fundamental principles of VLSI circuits and explore on the EDA platforms
- To learn the fundamental principles of Analog IC design and explore on the EDA platforms

LIST OF EXPERIMENTS

CYCLE – I FPGA BASED SYSTEM DESIGN

HDL based design entry and simulation of state machines. Synthesize, place and route, static timing analysis and critical path analysis

1. Design and Implementation of 16-bit ALU in FPGA using VHDL and Verilog
2. Design and implementation of a 32 - bit one hot ring – counter, up and down counter with Load and Preset functionality
3. Design of a barrel shifter using VHDL and Verilog
4. Implementation of ARM with FPGA
5. Implementing an 8x64 FIFO buffer with read and write ports of the FIFO operating at the same clock. Generate control signals to indicate the FIFO full/empty conditions
6. (a) State machine to detect any given sequence like '101' from an incoming serial stream
   (b) State machine to detect divisible by 5 value in an input serial stream of any length

CYCLE – II ANALOG IC DESIGN

Circuit Level Design and Post Layout-Simulation to analyse Frequency Response, Noise, Stability and Linearity of

7. Current Sources & Sinks, Current Mirrors/Amplifiers
8. Voltage & Current References, Bandgap Reference Circuits
9. Single Stage Amplifiers - Common Source Stage, Common Gate Stage, Source Follower
10. Cascade Amplifiers
11. Differential Amplifier with MOS Loads

TOTAL PERIODS: 60

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Create various logic modules in FPGA using VHDL and Verilog

CO2: Analysis the module with FPGA design flow

CO3: Understand and demonstrate complete design flow of basic VLSI circuits

CO4: Utilize ARM with FPGA

CO5: Explain design, simulation and analysis of signal integrity

CO6: Design circuit for real-time applications

COURSE CODE	COURSE TITLE	L	T	P	C
20AE112	TECHNICAL SEMINAR	0	0	2	1

OBJECTIVES:

- To understand the purpose of communication, in general, and technical communication, in particular
- To understand the importance of language skills in reading, listening and hence in making presentations
- To understand how the nature of intended audience, available time slot and the purpose of presentation can influence material preparation
- To learn to use at least one popular presentation software package, and to prepare clear slides
- To reflect on the possible ways of effective delivery, including handling questions

COURSE SCHEDULE	
Weeks 1 – 2	Introduction; Interactive discussions on the purpose and importance of communication
Weeks 3 – 4	Discussions on the importance of language skill in reading and listening, and of reflection; Reading and listening sessions
Weeks 5 – 6	Assessment 1: Oral exam on the above topics
Week 7	Tutorial and discussions on Microsoft Power Point
Weeks 8 – 9	Assessment 2: Presentation on a general topic
Week 10	Discussion on the fundamentals of technical presentations
Weeks 11 – 14	Assessment 3: Presentation on a technical topic
Week 15	Winding up

TOTAL PERIODS: 30

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Reflect on the purpose of communication, and on the ways of making effective presentations.

CO2: Explain the role language skill, reading and listening play in effective communication.

CO3: Make improved presentation on a topic from within their specialty.

CO4: Think critically and creatively to generate innovative and optimum solutions.

CO5: Present technical material orally with confidence and poise, including audiovisual materials.

CO6: Demonstrate use of appropriate methodologies, test the strength of their thesis statement.

REFERENCE BOOKS:

1. Ashraf Rizvi, M, Effective Technical Communication, Second Edition, Tata McGraw-Hill, New Delhi, 2017.
2. Mike Markel, Stuart A. Selber, Technical Communication, Twelfth Edition, Bedford Books, 2018.
3. Richard Johnson-Sheehan, Technical Communication Today, Sixth Edition, Pearson, 2017.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE201	DIGITAL CMOS VLSI DESIGN	3	0	0	3

OBJECTIVES:

- To introduce the basic concepts of MOS transistors.
- To introduce the basic concepts of CMOS Technologies.
- To provide a platform for transistor level digital circuits design.
- To learn and practice different logical implementation and their significances.
- To understanding of issues and tools related to ASIC design and implementation.

UNIT I MOSFET AND CMOS INVERTER 9

MOSFET: Device Structure and Physical Operation – Current-Voltage (I-V) Characteristics – Scaling – Non-ideal Features of MOS Transistors – MOSFET Capacitances – MOSFET SPICE Models CMOS Inverter: Circuit Operation - The Voltage-Transfer Characteristic - Dynamic Operation - Power Dissipation – Layout.

UNIT II CMOS PROCESSING TECHNOLOGY, DELAY AND POWER 9

CMOS Processing Technology: CMOS Technologies, Layout Design Rules, CMOS Process Enhancements.
Delay: Propagation Delays and Delay Models – Logic Effort - Path-Delay Optimization.
Power: Static Power Dissipation - Dynamic Power Dissipation - Power and Delay Trade-offs -Low-Power Designs.

UNIT III COMBINATIONAL LOGIC CIRCUIT DESIGN 9

Static CMOS Logic Circuits: NAND Gate – NOR Gate – Complex Logic Gates; Sizing Gates – Transmission Gate - Pseudo-nMOS Logic; Dynamic CMOS Logic Circuits: Basic Dynamic Logic – Non-ideal Effects of Dynamic Logic - Domino Logic.

UNIT IV SEQUENTIAL LOGIC CIRCUIT DESIGN AND DATA PATH SUB SYSTEMS DESIGN 9

Static Latches and Registers - Dynamic Latches and Registers - Alternative Register Styles, Pipelining - Nonbistable Sequential Circuits. Datapath Subsystem Designs: Architectures for Adders, Multipliers, Shifters.

UNIT V IMPLEMENTATION OPTIONS AND INTERCONNECT 9

Implementation Options: Platform based systems – ASICs – Field Programmable Devices – Design Flow Interconnect: RLC Parasitic, Interconnect Models – Parasitic Effects of Interconnects.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Design basic digital circuits in transistor level.
CO2: Analyze and choose suitable logical styles for a given problem.
CO3: Analyze and optimize the transistor level circuits.
CO4: Measure the delay, analyze and find the optimized delay.
CO5: Understand the issues involved in ASIC design including technology choice, design management and tool-flow.
CO6: Concepts of modeling a digital system using Hardware Description Language.

REFERENCE BOOKS:

1. Adel S. Sedra, Kenneth C. Smith, Microelectronic circuits, Oxford University Press, Seventh Edition, 2015.
2. Neil H. E. Weste, David Money Harris, CMOS VLSI Design: A Circuits and Systems Perspective, Pearson India, Fourth Edition, 2015.
3. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, Digital Integrated Circuits: A Design Perspective, Prentice Hall of India, Second Edition, 2003.
4. Ming-Bo Lin, Introduction to VLSI Systems: A Logic, Circuit, and System Perspective, CRC Press, 2012.
5. Sung-Mo Kang, Yusuf Leblebici, Chulwoo Kim, CMOS Digital Integrated Circuits: Analysis and Design, McGraw Hill Education, Fourth Edition, 2015.
6. Jacob Baker R, CMOS: Circuit Design, Layout and Simulation, Wiley Publications, Third Edition, 2012.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE202	HARDWARE – SOFTWARE CO-DESIGN	3	0	0	3

OBJECTIVES:

- To acquire the knowledge about system specification and modelling.
- To learn the formulation of partitioning
- To study the different technical aspects about prototyping and emulation
- To study the benefits of the co-design approach over current design process.
- To exploit the interaction of hardware and software with the goal to optimize and/or satisfy design constraints such as cost, performance, and power of the final product.

UNIT I SYSTEM SPECIFICATION AND MODELLING 9

Embedded Systems, Hardware/Software Co-Design, Co-Design for System Specification and Modeling, Co-Design for Heterogeneous Implementation - Single-Processor Architectures with one ASIC and many ASICs, Multi-Processor Architectures, Comparison of Co-Design Approaches, Models of Computation, Requirements for Embedded System Specification.

UNIT II HARDWARE / SOFTWARE PARTITIONING 9

The Hardware/Software Partitioning Problem, Hardware-Software Cost Estimation, Generation of the Partitioning Graph, Formulation of the HW/SW Partitioning Problem, Optimization , HW/SW Partitioning based on Heuristic Scheduling, HW/SW Partitioning based on Genetic Algorithms

UNIT III HARDWARE / SOFTWARE CO-SYNTHESIS 9

The Co-Synthesis Problem, State-Transition Graph, Refinement and Controller Generation, Co-Synthesis Algorithm for Distributed System- Case Studies with any one application.

UNIT IV PROTOTYPING AND EMULATION 9

Introduction, Prototyping and Emulation Techniques, Prototyping and Emulation Environments, Future Developments in Emulation and Prototyping, Target Architecture- Architecture Specialization Techniques, System Communication Infrastructure, Target Architectures and Application System Classes, Architectures for Control-Dominated Systems, Architectures for Data-Dominated Systems.

UNIT V DESIGN SPECIFICATION AND VERIFICATION 9

Concurrency, Coordinating Concurrent Computations, Interfacing Components, Verification, Languages for System-Level Specification and Design System-Level Specification, Design Representation for System Level Synthesis, System Level Specification Languages, Heterogeneous Specification and Multi-Language Co- simulation.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Assess prototyping and emulation techniques.
CO2: Understand various co-synthesis approaches.
CO3: Formulate the design specification and validate its functionality by simulation.
CO4: Identify the portioning solution based on the algorithms.
CO5: Propose an alternate design solution based on constraint analysis.
CO6: Analyze about the hardware and software integration.

REFERENCE BOOKS:

1. Giovanni De Micheli, Rolf Ernst Morgon, Reading in Hardware/Software Co-Design, Kaufmann Publishers, 2001.
2. Jorgen Staunstrup, Wayne Wolf, Hardware/Software Co-Design: Principles and Practice, Kluwer Academic Publication, 1997.
3. Ralf Niemann, Hardware/Software Co-Design for Data Flow Dominated Embedded Systems, Kluwer Academic Publication, 1998.
4. Koen Bertels, Koen Bertels, Hardware/Software Co-design for Heterogeneous Multi-core Platforms, Springer Netherlands, 2012.
5. Patrick R. Schaumont, A Practical Introduction to Hardware/Software Codesign, Second Edition, Springer, 2010.
6. Ti-Yen Yen, Wayne Wolf, Hardware-Software Co-Synthesis of Distributed Embedded Systems, Springer Science, 1996.

NPTEL: https://nptel.ac.in/courses/106/105/106105165/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE203	IoT SYSTEM DESIGN AND SECURITY	3	0	0	3

OBJECTIVES:

- To understand the basics of IoT.
- To get an idea about the various services provided by IoT.
- To familiarize themselves with various communication techniques.
- To get an idea of some application area where IoT can be applied.

- To understand the various issues in IoT.

UNIT I INTRODUCTION TO INTERNET OF THINGS 9

Rise of the machines – Evolution of IoT – Web 3.0 view of IoT – Definition and characteristics of IoT – Physical design of IoT – Logical design of IoT – IoT enabling technologies – IoT levels and deployment templates – A panoramic view of IoT applications.

UNIT II ARCHITECTURE OF IoT 9

Identification and Access to objects and services in the IoT environment(Current technologies for IoT naming-Solutions proposed by research projects-Research and Future development trends and forecast) – Middleware technologies for IoT system (IoT Ecosystem Overview – Horizontal Architecture Approach for IoT Systems-SOA-based IoT Middleware)Middleware architecture of RFID,WSN,SCADA,M2M–Challenges Introduced by 5G in IoT Middleware(Technological Requirements of 5G Systems-5G-based IoT Services and Applications Requirements-5G-based Challenges for IoT Middleware) - Perspectives and a Middleware Approach Toward 5G (COMPaaS Middleware) – Resource management in IoT

UNIT III SECURITY CONSIDERATIONS IN IoT SMART AMBIENT SYSTEMS 9

Security in Smart Grids and Smart Spaces for Smooth IoT Deployment in 5G (5G and the Internet of Things-Smart Spaces-Smart Grids Security and Privacy - Services that Need to Be Secure - Security Requirements -Security Attacks-Security Measures and Ongoing Research) - Security Challenges in 5G-Based IoT Middleware Systems(Security in 5G-Based IoT Middleware-Security Challenges Toward 5G).

UNIT IV IoT ENABLERS AND THEIR SECURITY AND PRIVACY ISSUES 9

Internet of Things layer wise Protocols and Standards- EPC global(architecture, specifications, industry adaptation, security and vulnerabilities, advantages and disadvantages)-Wireless HART-Zigbee- Near Field Communication- 6LoWPAN-Dash7-Comparative Analysis

UNIT V APPLICATIONS AND CASE STUDIES 9

Home automations - Smart cities – Environment – Energy – Retail – Logistics – Agriculture – Industry - Health and life style – Case study.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Articulate the main concepts, key technologies, strength and limitations of IoT.
CO2: Identify the architecture, infrastructure models of IoT.
CO3: Analyze the core issues of IoT such as security, privacy and interoperability.
CO4: Analyze and design different models for network dynamics.
CO5: Identify and design the new models for market strategic interaction.
CO6: Demonstrate the real time applications using IoT protocols and software

REFERENCE BOOKS:

1. Hobo Zhou, Internet of Things in the cloud: A middleware perspective, CRC press 2012.
2. Vijay Madisetti and Arshdeep Bahga, Internet of Things (A Hands-on Approach), VPT, First Edition, 2014.
3. Constandinos X. Mavromoustakis, George Mastorakis, Jordi Mongay Batalla, Internet of Things (IoT) in 5G Mobile Technologies, Springer International Publishing, Switzerland, 2016.

4. Dieter Uckelmann, Mark Harrison, Florian Michahelles, Architecting the Internet of Things, Springer-Verlag Berlin Heidelberg, 2011.
5. http://www.cse.wustl.edu/~jain/cse570-15/ftp/iot_prot/index.html.
6. Alasdair Gilchrist, IoT security Issues, Oreilly Publications, 2017.

NPTEL: https://nptel.ac.in/courses/106/105/106105166/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE211	ANALOG AND DIGITAL CMOS VLSI DESIGN LABORATORY	0	0	4	2

OBJECTIVES:

- To understand operation of NMOS and PMOS devices.
- To get familiar with the small- and large-signal models of NMOS and PMOS transistors.
- To understand the concept of gain and Transconductance of Transistors.
- Students will carry out a detailed analog circuit design starting with transistor characterization and finally realizing an IA design.
- At various stages of design, a typical state of art CAD VLSI tool will be used in various phases of experiments designed to bring out the key aspects of each important module in the CAD tool including the simulation, layout, LVS and parasitic extracted simulation.

List of Experiments:

1.Extraction of process parameters of CMOS process transistors

a. Plot ID vs. VGS at different drain voltages for NMOS, PMOS.
b. Plot ID vs. VGS at particular drain voltage (low) for NMOS, PMOS and determine Vt.
c. Plot log ID vs. VGS at particular gate voltage (high) for NMOS, PMOS and determine IOFF and sub-threshold slope.
d. Plot ID vs. VDS at different gate voltages for NMOS, PMOS and determine Channel length modulation factor.
e. Extract V_{th} of NMOS/PMOS transistors (short channel and long channel). Use VDS of appropriate voltage to extract V_{th} use the following procedure.

i. Plot gm vs VGS using SPICE and obtain peak gm point.

ii. Plot y=ID/(gm) as a function of VGS using SPICE.

iii. Use SPICE to plot tangent line passing through peak gm point in y (VGS)

f. Plot ID vs. VDS at different drain voltages for NMOS, PMOS, plot DC load line and calculate gm, gds, gm/gds, and unity gain frequency. Tabulate result according to technologies and comment on it

2. CMOS inverter design and performance analysis

a. i. Plot VTC curve for CMOS inverter and thereon plot dVout vs. dVin and determine transition voltage and gain g. Calculate VIL, VIH, NMH, NML for the inverter.

ii Plot VTC for CMOS inverter with varying VDD.

iii. Plot VTC for CMOS inverter with varying device ratio.

b. Perform transient analysis of CMOS inverter with no load and with load and determine tpHL, tpLH, 20%-to-80% tr and 80%-to-20% tf.

c. Perform AC analysis of CMOS inverter with fanout 0 and fanout 1.

3. Use spice to build a three stage and five stage ring oscillator circuit and compare its frequencies. Use FFT and verify the amplitude and frequency components in the spectrum.

4. Single stage amplifier design and performance analysis

a. Draw small signal voltage gain of the minimum-size inverter in the technology chosen as a function of input DC voltage. Determine the small signal voltage gain at the switching point using spice and compare the values for two different process transistors

b. Consider a simple CS amplifier with active load, with NMOS transistor as driver and PMOS transistor as load.

i. Establish a test bench to achieve VDSQ=VDD/2.

ii. Calculate input bias voltage for a given bias current.

iii. Use spice and obtain the bias current. Compare with the theoretical value

iv. Determine small signal voltage gain, -3dB BW and GBW of the amplifier using small signal analysis in spice, considering load capacitance.

v. Plot step response of the amplifier with a specific input pulse amplitude. Derive time constant of the output and compare it with the time constant

5.Three OPAMP Instrumentation Amplifier.

Use proper values of resistors to get a three OPAMP INA with differential-mode voltage gain=10. Consider voltage gain=2 for the first stage and voltage gain=5 for the second stage.

a. Draw the schematic of op-amp macro model.

b. Draw the schematic of INA.

c. Obtain parameters of the op-amp macro model such that it meets a given specification for:

i. low-frequency voltage gain,

ii. unity gain BW (fu),

iii. input capacitance

iv. output resistance,

v. CMRR

d.Draw schematic diagram of CMRR simulation setup

e. Simulate CMRR of INA using AC analysis (it's expected to be around 6dB below CMRR of OPAMP).

f. Plot CMRR of the INA versus resistor mismatches (for resistors of second stage only) changing from -5% to +5% (use AC analysis). Generate a separate plot for mismatch in each resistor pair. Explain how CMRR of OPAMP changes with resistor mismatches

g. Repeat (iii) to (vi) by considering CMRR of all OPAMPs with another low frequency gain setting

6. Use Layout editor.

a. Draw layout of a minimum size inverter using transistor from CMOS process library

Use Metal 1 as interconnect line between inverters.

b. Run DRC, LVS and RC extraction. Make sure there is no DRC error.

c. Extract the netlist. Use extracted netlist and obtain tPHL tPLH for the inverter using Spice.

d. Use a specific interconnect length and connect and connect three inverters in a chain.

Extract the new netlist and obtain tPHL and tPLH of the middle inverter

e. Compare new values of delay times with corresponding values obtained in part 'c'.

7. Design a differential amplifier with resistive load using transistors from CMOS process library that meets a given specification for the following parameter

a. low-frequency voltage gain,

b. unity gain BW (fu),

c. Power dissipation

i. Perform DC analysis and determine input common mode range and compare with the theoretical values.

ii. Perform time domain simulation and verify low frequency gain.

iii. Perform AC analysis and verify.

TOTAL PERIODS: 60

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Design digital and analog Circuit using CMOS given a design specification

CO2: Design and carry out time domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

CO3: Design and carry out frequency domain simulations of simple analog building blocks, study the pole zero behaviors and compute the input/output impedances

CO4: Use EDA tools like Cadence, Mentor Graphics or other open source software tools like LTSpice

CO5: Explain the CMOS inverter design and performance analysis

CO6: Study of performance metrics of CMRR.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE212	MINI PROJECT AND TERM PAPER WRITING	0	0	2	2

OBJECTIVES:

In this course, students will develop their scientific and technical reading and writing skills that they need to understand and construct research articles. A term paper requires a student to obtain information from a variety of sources (i.e., Journals, dictionaries, reference books) and then place it in logically developed ideas. The work involves the following steps:

1. Selecting a subject, narrowing the subject into a topic
2. Stating an objective.
3. Collecting the relevant bibliography (at least 15 journal papers)
4. Preparing a working outline.
5. Studying the papers and understanding the author's contributions and critically analyzing each paper.
6. Preparing a working outline
7. Linking the papers and preparing a draft of the paper.
8. Preparing conclusions based on the reading of all the papers.
9. Writing the Final Paper and giving final Presentation

Please keep a file where the work carried out by you is maintained. Activities to be carried Out

Activity	Instructions	Submission week	Evaluation
Selection of area of interest and Topic	You are requested to select an area of interest, topic and state an objective	2nd Week	3 % Based on clarity of thought, current relevance and clarity in writing
Stating an Objective			
Collecting Information about your area & topic	1.List 1 Special Interest Groups or professional society 2. List 2 journals 3.List2 conferences, symposia or workshops 4. List 1 thesis title 5. List 3 web presences (mailing lists, forums, news sites) 6. List 3 authors who publish regularly in your area 7. Attach a call for papers (CFP) from your area.	3rd Week	3% (the selected information must be area specific and of international and national standard)
Collection of Journal papers in the topic in the context of the objective – collect 20 & then filter	▪ You have to provide a complete list of references you will be using- Based on your objective -Search various digital libraries and Google Scholar ▪ When picking papers to read - try to: ▪ Pick papers that are related to each other in some ways and/or that are in the same field so that you can write a meaningful survey out of them, ▪ Favour papers from well-known journals and conferences, ▪ Favour "first" or "foundational" papers in the field (as indicated in other people's survey paper), ▪ Favour more recent papers, ▪ Pick a recent survey of the field so you can quickly gain an overview, ▪ Find relationships with	4th Week	6% (the list of standard papers and reason for selection)

	respect to each other and to your topic area (classification scheme/categorization) ▪ Mark in the hard copy of papers whether complete work or section/sections of the paper are being considered.		
Reading and notes for first 5 papers	Reading Paper Process ▪ For each paper form a Table answering the following questions: ▪ What is the main topic of the article? ▪ What was/were the main issue(s) the author said they want to discuss? ▪ Why did the author claim it was important? ▪ How does the work build on other's work, in the author's opinion? ▪ What simplifying assumptions does the author claim to be making? ▪ What did the author do? ▪ How did the author claim they were going to evaluate their work and compare it to others? ▪ What did the author say were the limitations of their research? ▪ What did the author say were the important directions for future research? ▪ Conclude with limitations/issues not addressed by the paper (from the perspective of your survey)	5th Week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Reading and notes for next 5 papers	Repeat Reading Paper Process	6th Week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions

			about each paper)
Reading and notes for final 5 papers	Repeat Reading Paper Process	7th Week	8% (the table given should indicate your understanding of the paper and the evaluation is based on your conclusions about each paper)
Draft outline 1 and Linking papers	Prepare a draft Outline, your survey goals, along with a classification / categorization diagram	8th Week	8% (this component will be evaluated based on the linking and classification among the papers)
Abstract	Prepare a draft abstract and give a presentation	9th Week	6% (Clarity, purpose and conclusion) 6% Presentation & Viva Voce
Introduction Background	Write an introduction and background sections	10th Week	5% (clarity)
Sections of the paper	Write the sections of your paper based on the classification / categorization diagram in keeping with the goals of your survey	11th Week	10% (this component will be evaluated based on the linking and classification among the papers)
Your conclusions	Write your conclusions and future work	12th Week	5% (conclusions – clarity and your ideas)
Final Draft	Complete the final draft of your paper	13th Week	10% (formatting, English, Clarity and linking) 4% Plagiarism Check Report
Seminar	A brief 15 slides on your paper	14th& 15th Week	10% (based on presentation and Viva-voce)

TOTAL PERIODS: 30

COURSE CODE	COURSE TITLE	L	T	P	C
20AE301	ADVANCED DIGITAL IMAGE PROCESSING	3	0	0	3

OBJECTIVES:

- To understand the image fundamentals and mathematical transforms necessary for image Processing and to study the image enhancement techniques
- To understand the image segmentation and representation techniques.
- To understand how image are analyzed to extract features of interest
- To introduce the concepts of image registration and image fusion.
- To analyze the constraints in image processing when dealing with 3D data sets.

UNIT I FUNDAMENTALS OF DIGITAL IMAGE PROCESSING 9

Elements of visual perception, brightness, contrast, hue, saturation, Mach band effect, 2D Image transforms-DFT, DCT, KLT, and SVD. Image enhancement in spatial and frequency

domain, Review of morphological image processing.

UNIT II SEGMENTATION **9**

Edge detection, Thresholding, Region growing, Fuzzy clustering, Watershed algorithm, Active contour methods, and Texture feature based segmentation, Model based segmentation, Atlas based segmentation, Wavelet based Segmentation methods.

UNIT III FEATURE EXTRACTION **9**

First and second order edge detection operators, Phase congruency, Localized feature extraction-detecting image curvature, shape features Hough transform, shape skeletonization, Boundary descriptors, Moments, Texture descriptors- Autocorrelation, Co-occurrence features, Runlength features, Fractal model based features, Gabor filter, wavelet features.

UNIT IV REGISTRATION AND IMAGE FUSION **9**

Registration- Preprocessing, Feature selection-points, lines, regions and templates Feature correspondence-Point pattern matching, Line matching, region matching Template matching .Transformation functions-Similarity transformation and Affine Transformation. Resampling-Nearest Neighbour and Cubic Splines Image Fusion-Overview of image fusion, pixel fusion, Multiresolution based fusion discrete wavelet transform, Curvelet transform. Region based Fusion.

UNIT V 3D IMAGE VISUALIZATION **9**

Sources of 3D Data sets, Slicing the Data set, Arbitrary section planes, The use of color, Volumetric display, Stereo Viewing, Ray tracing, Reflection, Surfaces, Multiply connected surfaces, Image processing in 3D, Measurements on 3D images.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: To understand image formation and the role human visual system plays in perception of gray and color image data.

CO2: To apply image processing techniques in both the spatial and frequency (Fourier) domains.

CO3: To design image analysis techniques in the form of image segmentation and to evaluate the Methodologies for segmentation

CO4: To conduct independent study and analysis of feature extraction techniques.

CO5: To understand the concepts of image registration and image fusion.

CO6: To analyze the constraints in image processing when dealing with 3D data sets and to apply image processing algorithms in practical applications.

REFERENCE BOOKS:

1. Chris Solomon, Toby Breckon, Fundamentals of Digital Image Processing, Wiley, 2011.

2. Bernd Jahne, Practical Handbook on Image Processing for Scientific Applications, CRC Press, 2004.

3. Bernd Jahne, Digital Image Processing, Springer Berlin Heidelberg 2013.

4. Alan C. Bovik, Handbook of Image and Video Processing, Elsevier Science, 2010.

5. Scott E Umbaugh, Digital Image Processing and Analysis: Applications with MATLAB and CVIPtools, CRC Press, 2017.
6. John C. Russ, F. Brent Neal, The Image Processing Handbook, Seventh Edition, CRC Press, 2018.

NPTEL: https://nptel.ac.in/courses/117/105/117105135/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE121	RF TEST AND MEASUREMENT	3	0	0	3

OBJECTIVES:

- To design blocks for a test bench for different RF measurements
- To learn the basic elements of RF and microwave measurements and test processes.
- To plan ahead and select components and devices needed for your design testing
- To understand the different causes of measurement uncertainty, and how they can be quantified.
- To analyze different measurement problems and, based on the analysis select the appropriate method.

UNIT I INTRODUCTION TO RF TESTING **9**

Fundamentals of transmission lines and its models – Scattering Parameters - Characteristics of RF Signal – Mismatches - Fixture loss performance and measurement Accuracy-Microwave probing.

UNIT II RF POWER MEASUREMENT **9**

Importance of RF Power measurement – Units and Definitions - Methods of sensing Power-Thermistors Sensors: Instrumentation-Thermocouple Sensors – Diode Sensors, Power meters – Measurement Uncertainty – Parameter for Instrumentation: Accuracy, Range, SWR, Speed of Response, Susceptibility to overload, Signal waveform.

UNIT III RF ANALYZERS **9**

Signal Generator – Spectrum Analysis using FT- VNA Technology: Sources, Switches, converters, Directional devices, IF sections – Measurements in VNA: Gain, Delay, NF, Load pull, Antenna measurements, Materials measurements – Cables and Connectors – Temperature dependence, Measurement location.

UNIT IV ANTENNA MEASUREMENT **9**

Antenna radiation pattern arrangement – Ranges – Amplitude and Phase measurement – Gain Measurements: Two antenna, Three antenna, Gain Transfer methods – Directivity measurements – Impedance Measurements – Polarization measurements – Scale Model Antenna Measurements.

UNIT V EMIC MEASUREMENT **9**

Conducted EMI Testing: LISN, High Impedance voltage probes, inductively coupled current injection and magnetic field probes - RE Testing: Wideband antennas and Dipoles for RE testing, Radiated Immunity requirements, TEM and GTEM Cell testing for RI, EMC Testing in screened chambers, ESD and NEMP testing methods.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Understand the basics of RF measurement and related parameters associated with measurements.

CO2: Understand the instrumentation of measuring devices.

CO3: Evaluate the performance of samples such as Antennas and RF components.

CO4: Understand the management of various test processes for EMI/EMC.

CO5: Understand and identify the correct measurement technique and procedure for RF testing.

CO6: Gain knowledge about the RFID technology

REFERENCE BOOKS:

1. Teppati V, Ferrero A, & Sayed M. (Eds.). Modern RF and Microwave Measurement Techniques, Cambridge University Press, 2013.
2. Agilent's, Fundamentals of RF and Microwave Power Measurements: Application Note 64 -11B, 2006.
3. Constantine A. Balanis, Antenna Theory: Analysis and Design, Wiley, Fourth Edition, 2016.
4. Morgan, David, A Handbook for EMC Testing and Measurement, IET Electrical Measurement, 2007.
5. Joseph C, Practical Radio Frequency Test and Measurement: A Technician's Handbook, Newnes (Elsevier), 2002.
6. Protap Pramanick, Prakash Bhartia, Modern RF and Microwave Filter Design, Artech, 2016.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE122	DSP PROCESSOR ARCHITECTURE AND PROGRAMMING	3	0	0	3

OBJECTIVES:

- To study the fundamentals of programmable digital signal processors.
- To Acquire knowledge of DSP computational building blocks and knows how to achieve speed in DSP architecture or processor.
- To introduce the development tools required to program the DSP processors.
- To study the latest programmable DSPs from various vendors.
- To implement and demonstrate signal processing algorithms in the programmable DSPs.

UNIT I FUNDAMENTALS OF PROGRAMMABLE DSPs **9**

Basic elements of a digital signal processing (DSP) system – Architectural requirement of a PDSPs – Different architectures of PDSPs – Common features of PDSPs – Multiplier - Multiplier and Accumulator (MAC) – Shifter - On-chip memories – On-chip peripherals for external interfacing and speed issues.

UNIT II DEVELOPMENT TOOLS FOR PDSPs **9**

Introduction – DSP development system – DSP starter kits (DSKs) – Code Composer Studio (CCS) – Assembler - C/C++ Compiler – Linker and memory allocation – Support files – Chip support library (CSL) – Board support library (BSL) – Run-time support library (RTS) – Programming examples to

test the DSK tools.

UNIT III TMS320C5X DSP PROCESSOR **9**

Architectural overview of TMS320C5X (C5X) DSP processor – Central processing unit – internal memory organization – Serial port – Hardware Timer – Direct memory access (DMA) controller – Assembly language syntax – Addressing modes – Assembly language instructions – Programming examples for real-time signal processing applications.

UNIT IV TMS320C6X DSP PROCESSOR **9**

Architecture of the TMS320C6X (C6X) DSP processor – Functional units – Registers – Timers – Interrupts – Direct memory access – Multichannel buffered serial ports – Special addressing modes – Instruction set – Assembler directives – Linear assembly - Programming examples for real-time signal processing applications.

UNIT V ADSP AND MOTOROLA DSP PROCESSORS **9**

Architecture of the ADSP 210XX and Blackfin 50X series of DSP processors – Addressing modes – Assembly language instructions – Architecture of Motorola DSP563XX DSP processor – Comparison of the features of DSP family processors.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Explain the architecture and operation of DSP Processors.

CO2: Infer knowledge on development tools for PDSPs.

CO3: Understand the hardware/software tradeoffs involved in the design of DSP Processors.

CO4: Infer about the control instructions, interrupts and instruction sets for TMS processors.

CO5: Create and analyses a simple DSP based System using ADSP and MOTOROLA Processors.

CO6: Illustrate the features of on-chip peripheral devices and its interfacing along with its programming details

REFERENCE BOOKS:

1. Avtar Singh and S. Srinivasan, Digital Signal Processing – Implementations using DSP Microprocessors with Examples from TMS320C54xx, Cengage Learning India Private Limited, Delhi 2012.
2. B.Venkataramani and M.Bhaskar, Digital Signal Processors – Architecture, Programming and Applications, Tata McGraw – Hill Publishing Company Limited. New Delhi, 2003.
3. Rulph Chassaing, Digital Signal Processing and Applications with the C6713 and C6416 Dsk, A John Wiley & Sons, Inc., Publication, 2012.
4. Lapsley, et_al., DSP Processor Fundamentals, Architectures & Features", S. Chand & Co, 2000.
5. Jonatham Stein, Digital Signal Processing, John Wiley, 2000.
6. User guides Texas Instrumentation, Analog Devices, Motorola.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE123	COMPUTER ARCHITECTURE AND PARALLEL PROCESSING	3	0	0	3

OBJECTIVES:

- To understand the difference between pipeline and parallel processing concepts.
- To analyze and identify the conditions of parallelism.
- To study the different multi core architectures.
- To study various types of processor architectures and the importance of scalable architectures.
- To study Memory Architectures, Memory Technology and Optimization.

UNIT I COMPUTER DESIGN AND PERFORMANCE MEASURES 9

Fundamentals of Computer Design – Parallel and Scalable Architectures – Multiprocessors –Multi-vector and SIMD architectures – Multithreaded architectures – Stanford Dash multiprocessor – KSR1 - Data-flow architectures - Performance Measures.

UNIT II PARALLEL PROCESSING, PIPELINING AND ILP 9

Instruction Level Parallelism and Its Exploitation - Concepts and Challenges - Pipelining processors - Overcoming Data Hazards with Dynamic Scheduling – Dynamic Branch Prediction - Speculation - Multiple Issue Processors - Performance and Efficiency in Advanced Multiple Issue Processors.

UNIT III MEMORY HIERARCHY DESIGN 9

Memory Hierarchy - Memory Technology and Optimizations – Cache memory – Optimizations of Cache Performance – Memory Protection and Virtual Memory - Design of Memory Hierarchies.

UNIT IV MULTIPROCESSORS 9

Symmetric and distributed shared memory architectures – Cache coherence issues – Performance Issues – Synchronization issues – Models of Memory Consistency - Interconnection networks – Buses, crossbar and multi-stage switches.

UNIT V MULTI-CORE ARCHITECTURES 9

Software and hardware multithreading – SMT and CMP architectures – Design issues – Case-studies – Intel Multi-core architecture – SUN CMP architecture – IBM cell architecture – hp architecture.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Explain design of memory hierarchies.

CO2: List the techniques for exploiting of instruction-level parallelism.

CO3: Evaluate the performance Issues and Synchronization issues.

CO4: Study the maintenance of cache coherence.

CO5: Compare multicore architectures.

CO6: Distinguish the performance of pipelining and non-pipelining environment in a processor

REFERENCE BOOKS:

1. David E. Culler, Jaswinder Pal Singh, Parallel Computing Architecture: A hardware/ software approach, Morgan Kaufmann / Elsevier, 1997.
2. Dimitrios Soudris, Axel Jantsch, Scalable Multi-core Architectures: Design Methodologies and Tools, Springer, 2012.

3. Hwang Briggs, Computer Architecture and parallel processing, McGraw Hill, 2017.
4. John L. Hennessey and David A. Patterson, Computer Architecture – A quantitative approach, Morgan Kaufmann / Elsevier, Fourth Edition, 2007.
5. John P. Hayes, Computer Organization and Architecture: Designing for Performance, Pearson, 2013.
6. William Stallings, Computer Organization and Architecture – Designing for Performance, Pearson Education, Seventh Edition, 2006.

NPTEL: https://nptel.ac.in/courses/106/103/106103183/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE124	ELECTROMAGNETIC INTERFERENCE AND COMPATIBILITY	3	0	0	3

OBJECTIVES:

- To understand the basics of EMI and EMI sources.
- To understand EMI Problems.
- To understand Measurement Technique for Emission.
- To impart comprehensive insight about the current EMC standards.
- To provide an insight into various techniques and procedures required for the design of electronic systems, which are in compliance with the EMC guidelines.

UNIT I BASIC THEORY **9**

Introduction to EMI and EMC, Intra and inter system EMI, Elements of Interference, Sources and Victims of EMI, Conducted and Radiated EMI emission and susceptibility, Case Histories, Radiation hazards to humans, Various issues of EMC, EMC Testing categories EMC Engineering Application.

UNIT II COUPLING MECHANISM **9**

Electromagnetic field sources and Coupling paths, Coupling via the supply network, Common mode coupling, Differential mode coupling, Impedance coupling, Inductive and Capacitive coupling, Radioactive coupling, Ground loop coupling, Cable related emissions and coupling, Transient sources, Automotive transients.

UNIT III EMI MITIGATION TECHNIQUES **9**

Working principle of Shielding and Murphy's Law, LF Magnetic shielding, Apertures and shielding effectiveness, Choice of Materials for H, E, and free space fields, Gasketing and sealing, PCB Level shielding, Principle of Grounding, Isolated grounds, Grounding strategies for Large systems, Grounding for mixed signal systems, Filter types and operation, Surge protection devices, Transient Protection.

UNIT IV STANDARD AND REGULATION **9**

Need for Standards, Generic/General Standards for Residential and Industrial environment, Basic Standards, Product Standards, National and International EMI Standardizing Organizations; IEC, ANSI, FCC, AS/NZS, CISPR, BSI, CENELEC, ACEC. Electro Magnetic Emission and susceptibility standards and specifications, MIL461E Standards.

UNIT V EMI TEST METHODS AND INSTRUMENTATION 9

Fundamental considerations, EMI Shielding effectiveness tests, Open field test, TEM cell for immunity test, Shielded chamber, Shielded anechoic chamber, EMI test receivers, Spectrum analyzer, EMI test wave simulators, EMI coupling networks, Line impedance stabilization networks, Feed through capacitors, Antennas, Current probes, MIL -STD test methods, Civilian STD test methods.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Understand the various sources of Electromagnetic interference.
CO2: Identify Standards.
CO3: Compare EMI test methods.
CO4: Discuss EMI mitigation techniques.
CO5: Understand and differentiate the various EMC pre compliance measurement.
CO6: Diagnose and solve basic electromagnetic compatibility problems

REFERENCE BOOKS:

1. Bemhard Keiser, Principles of Electromagnetic Compatibility, Third Edition, Artech House, Norwood, 1986.
2. Clayton Paul, Introduction to Electromagnetic Compatibility, Wiley Interscience, 200.6
3. Dr Kenneth L Kaiser, The Electromagnetic Compatibility Handbook, CRC Press 2005.
4. Norman Violette, Electromagnetic Compatibility, Springer, 2013.
5. Donald R. J., Electromagnetic Interference and Compatibility: Electrical noise and EMI specifications Volume 1 of A Handbook Series on Electromagnetic Interference and Compatibility, White Publisher-Don white consultants Original from the University of Michigan Digitized 6 Dec 2007.
6. Henry W. Ott, Electromagnetic Compatibility Engineering, John Wiley & Sons Inc, Newyork, 2009.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE221	RECONFIGURABLE VLSI ARCHITECTURE	3	0	0	3

OBJECTIVES:

- To learn designing using HDLs in FPGA platforms
- To understand the concept, device and system architecture of reconfigurable computing systems.
- To understand the different types of compute models for programming reconfigurable architectures.
- To understand the concepts of architecture reconfigurability, programmable logic devices and optimization of the Reconfigurable computer architecture to the task algorithm and data structure.
- To expose the students to HDL programming and familiarize with the system development environment.

UNIT I INTRODUCTION **9**

General Purpose Computing, Domain-specific processors, Application specific processors, Reconfigurable Computing Systems, Fields of Application – Evolution of reconfigurable systems – Classification of reconfigurable architecture - Fine, coarse grain and hybrid architectures – Examples.

UNIT II RECONFIGURABLE HARDWARE TECHNOLOGIES **9**

FPGAs - ALTERA Stratix ALTERA Cyclone, Xilinx Virtex, Xilinx Spartan. IC Devices with Embedded Reconfigurable Resources – ATMEL FPSLICs, Quicksilver ADAPT2000, IPflex DAPDNA-2 processor Motorola MRC6011, Pico Chip PC102, Leopard Logic Gladiator CLD - Embedded Reconfigurable Cores.

UNIT III PROGRAMMING RECONFIGURABLE SYSTEMS **9**

Compute Models, System Architectures - Programming FPGA Applications in HDL – Compiling C for Spatial Computing – Operating System Support for Reconfigurable Computing.

UNIT IV HIGH LEVEL DESIGN **9**

Synthesis: FPGA Design flow, Design Environment and Constraints, Logic Synthesis. Verification: Functional Verification, Simulation, Test Bench Design, Timing Analysis. Placement, Routing, Configuration Bit-stream Generation. Case Study: FPGA Based Design Flow.

UNIT V HIGH LEVEL DESIGN **9**

System on a Programmable Chip (SoPC) Designs - Design Flow for Reconfigurable Systems-On-Chip - Design Cases.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Understand and identify the need for reconfigurable architecture.

CO2: Understand and discuss the various architecture of reconfigurable computing systems.

CO3: Explain the operating system support for reconfigurable computing.

CO4: Design and Develop applications using Hardware Description Language and appropriate.

CO5: Design and develop Reconfigurable Systems-On-Chip.

CO6: Explain the routing process and describe the optimization techniques for technology independent designs and use of RCAs in ASIC design

REFERENCE BOOKS:

1. Christophe Bobda, Introduction to Reconfigurable Computing – Architectures, Algorithms and Applications, Springer, 2010.
2. Nikolaos S. Voros and Konstantinos Masselos, System Level Design of Reconfigurable Systems-On-Chip, Springer, 2005.
3. Scott Hauck and Andre Dehon (Eds.), Reconfigurable Computing – The Theory and Practice of FPGA-Based Computation, Elsevier / Morgan Kaufmann, 2008.
4. Ming-Bo Lin, Digital System Designs and Practices - Using Verilog HDL and FPGAs, John Wiley & Sons, 2008.
5. Maya B. Gokhale and Paul S. Graham, Reconfigurable Computing: Accelerating Computation with Field-Programmable Gate Arrays, Springer, 2005.
6. Lev Kirischian, Reconfigurable Computing System Engineering, CRC Press, 2016.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE222	NANO ELECTRONICS AND TECHNOLOGY	3	0	0	3

OBJECTIVES:

- To understand the basic modelling of quantum mechanics.
- To understand various advanced concepts in nanoelectronics.
- To understand the synthesis of Nano materials.
- To understand the characterization methods of Nano materials.
- To understand Nano electronic devices and their applications.

UNIT I FUNDAMENTALS OF NANO ELECTRONICS AND NANO TECHNOLOGY **9**

Top down approach - Bottom up approach - Scaling to Nano, Particles and waves - Quantum mechanics - Time independent Schrodinger wave equation - Quantum dots - Wires and Well.

UNIT II NANO MATERIALS SYNTHESIS **9**

Introduction and basic properties of Nanomaterials - Methods to produce nanomaterials, Sol gel method - Applications of Nanomaterials - Synthesis and application of Carbon Nano materials - Carbon Nano cones, and nanowires - Nano composites.

UNIT III NANO MATERIALS SYNTHESIS **9**

Optical microscopy - Scanning electron microscopy - Transmission electron microscopy - Atomic force microscopy - Scanning tunnelling microscopy-X-Ray Diffraction.

UNIT IV NANO ELECTRONIC SENSORS AND DEVICES **9**

Single electron transistors - Carbon nanotube FETs and SETs - Semiconductor nanowire FETs and SETs - Molecular SETs and molecular electronics - Quantum well infrared photo detectors.

UNIT V APPLICATIONS OF NANOTECHNOLOGY **9**

Nano technology for Energy- Solar cells, Fuel cells - Nano technology in drug delivery - Nanotechnology in communication - Nanotechnology in cosmetics - Tissue engineering - Agriculture and food industry.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Understand the basics and the theoretical foundations of Nano electronics.

CO2: Obtain the knowledge of Single Electron Devices and carbon based nano electronic devices.

CO3: Understand the use of synthesis methods and describe the properties of Nanomaterials.

CO4: Analyze the key performance aspects of Nano electronic devices and its characterization.

CO5: Understand the applications of nanotechnology.

CO6: Design and simulate various advanced nanoelectronic devices

REFERENCE BOOKS:

1. Murty.B.S, Shankar.P, Baldev Raj, Rath B.B, James Murday, Textbook of Nanoscience and Nanotechnology, Springer, Universities press, 2012.
2. Fluker M.H, Nanotechnology: Importance and Applications, IK International Publishing, 2010.
3. Wesley Crowell Sanders, Basic Principles of Nanotechnology, CRC Press, Taylor & Francis, 2018.
4. Murty B.S, Shankar P, Raj B, Rath B.B, Murday J, Textbook of Nanoscience and

Nanotechnology, Springer publishing, 2013.

5. Raja K S and M Kannan Subramanian, Textbook on Fundamentals and Applications of Nanotechnology (PB), Tamil Nadu Agricultural University, 2018.
6. Rainer Waser, Nanoelectronics and Information Technology: Advanced Electronic Materials and Novel Devices, Wiley, 2012.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE223	PROGRAMMING LANGUAGES FOR EMBEDDED SOFTWARE	3	0	0	3

OBJECTIVES:

- To make students familiar with the basic concepts embedded software.
- To foster ability to understand the design concept of object-oriented programming techniques.
- To introduce the concept of integrating hardware and software for microcontroller application systems.
- To explain programming concepts and embedded programming in c and C++.
- Ability to understand the role of scripting languages in embedded software.

UNIT I EMBEDDED 'C' 9

Programming Bitwise operations, Dynamic memory allocation, OS services Linked list, stack and queue, Sparse matrices, Binary tree. Interrupt handling in C, Code optimization issues. Writing LCD drives, LED drivers, Drivers for serial port communication. Embedded Software Development Cycle & Methods (Waterfall, Agile).

UNIT II OBJECT ORIENTED PROGRAMMING 9

Introduction to procedural, modular, object-oriented and generic programming techniques, Limitations of procedural programming, objects, classes, data members, methods, data encapsulation, data abstraction and information hiding, inheritance, polymorphism.

UNIT III CPP PROGRAMMING 9

'cin', 'cout', formatting and I/O manipulators, new and delete operators, Defining a class, data members and methods, 'this' pointer, constructors, destructors, friend function, dynamic memory allocation.

UNIT IV OVERLOADING AND INHERITANCE 9

Need of operator overloading, overloading the assignment, overloading using friends, type conversions, single inheritance, base and derived classes, friend classes, types of inheritance, hybrid inheritance, multiple inheritance, virtual base class, polymorphism, virtual functions.

UNIT V TEMPLATES 9

Function template and class template, member function templates and template arguments, Exception Handling: syntax for exception handling code: try-catch- throw, Multiple Exceptions. Scripting Languages: Overview of Scripting Languages – PERL, CGI, VB Script, Java Script. PERL.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Write an embedded C application of moderate complexity.

CO2: Develop and analyze algorithms in C++.
CO3: Differentiate interpreted languages from compiled languages.
CO4: Develop I/O Management.
CO5: Understand the concept of overloading and inheritance in embedded C.
CO6: Develop and test the programs using application specific scripting languages

REFERENCE BOOKS:

1. Michael J. Pont , Embedded C, Pearson Education, Second Edition, 2008.
2. Randal L. Schwartz, Learning Perl, O'Reilly Publications, Sixth Edition 2011.
3. A. Michael Berman, Data structures via C++, Oxford University Press, 2002.
4. Robert Sedgewick, Algorithms in C++, Addison Wesley Publishing Company, 1999.
5. Abraham Silberschatz, Peter B, Greg Gagne, Operating System Concepts, John Willey & Sons, 2005.
6. Wayne Wolf, Computers as Components-principles of Embedded Computer system Design, First Edition, Elseveir, 2009.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE224	ADVANCED MICROPROCESSORS AND MICROCONTROLLERS ARCHITECTURES	3	0	0	3

OBJECTIVES:

- To familiarize about the features, specification and features of modern microprocessors.
- To understand the features of advanced microprocessors.
- To gain knowledge about the architecture of Intel 32and 64-bit microprocessors and features associated with them.
- To familiarize about the features, specification and features of modern microcontrollers.
- To gain knowledge about the 32-bit microcontrollers based on ARM and PIC32 architectures.

UNIT I FEATURES OF MODERN MICROPROCESSORS 9

Evolution of microprocessors - Data and Address buses – clock speed – memory interface - multi-core architectures – cache memory hierarchy – operating modes – super scaler execution – dynamic execution – over clocking – integrated graphics processing - performance benchmarks.

UNIT II HIGH PERFORMANCE CISC ARCHITECTURES 9

Introduction to IA 32 bit architecture – Intel Pentium Processors family tree – Memory Management – Branch prediction logic - Superscalar architecture – Hyper threading technology – 64 bit extension technology – Intel 64 bit architecture - Intel Core processor family tree – Turbo boost technology – Smart cache - features of Nehalem microarchitecture.

UNIT III HIGH PERFORMANCE RISC ARCHITECTURE - ARM 9

RISC architecture merits and demerits – The programmer's model of ARM Architecture – 3-stage pipeline ARM organization - 3-stage pipeline ARM organization – ARM instruction execution – Salient features of ARM instruction set - ARM architecture profiles (A, R and M profiles).

UNIT IV FEATURES OF MODERN MICROPROCESSORS **9**

Introduction to microcontrollers – microcontroller vs microprocessors – microcontroller architecture - Processor Core – Memory interfaces– Communication interfaces (SPI,I^2C, USB and CAN) – ADC - PWM – Watchdog timers – Interrupts – Debugging interfaces.

UNIT V HIGH PERFORMANCE MICROCONTROLLER ARCHITECTURES **9**

Introduction to the Cortex-M Processor Family - ARM 'Cortex-M3' architecture for microcontrollers – Thumb 2 instruction technology – Internal Registers - Nested Vectored Interrupt controller - Memory map - Interrupts and exception handling – Applications of Cotex-M3 architecture.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Explain the features and important specifications of modern microprocessors.

CO2: Explain the salient features CISC microprocessors based on IA-32 bit and IA-64 bit architectures.

CO3: Explain the salient features RISC processors based on ARM architecture and different application profiles of ARM core.

CO4: Explain the features and important specifications of modern microcontrollers.

CO5: Explain about ARM – M3 architecture and its salient features.

CO6: Explain the architecture of generic advanced microprocessor and features of advanced microprocessors

REFERENCE BOOKS:

1. Barry. B. Breg, the Intel Microprocessors, Eighth Edition, Pearson Prentice Hal, 2009.
2. Gene .H.Miller, Micro Computer Engineering, Third Edition, Pearson Education, 2003.
3. Intel Inc, Intel 64 and IA-32 Architectures Developer's Manual, Volume-I, 2016.
4. Joseph Yiu, The Definitive Guide to the ARM ® Cortex-M3, Newnes, 2010.
5. Steve Furber, ARM System –On –Chip architecture, Second Edition, Wesley, 2000.
6. Trevor Martin, The Designer's Guide to the Cortex-M Processor Family, Newness, 2013.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE225	WIRELESS ADHOC AND SENSOR NETWORKS	3	0	0	3

OBJECTIVES:

- To understand the basics of Ad-hoc & Sensor Networks.
- To learn various fundamental and emerging protocols of all layers.
- To study about the issues pertaining to major obstacles in establishment and efficient management of Ad-hoc and sensor networks.
- To understand the nature and applications of Ad-hoc and sensor networks.
- To understand various security practices and protocols of Ad-hoc and Sensor Networks.

UNIT I MAC & TCP IN AD HOC NETWORKS **9**

Fundamentals of WLANs – IEEE 802.11 Architecture - Self configuration and Auto configuration-Issues in Ad-Hoc Wireless Networks – MAC Protocols for Ad-Hoc Wireless

Networks – Contention Based Protocols - TCP over Ad-Hoc networks-TCP protocol overview - TCP and MANETs – Solutions for TCP over Ad-Hoc Networks.

UNIT II ROUTING IN AD HOC NETWORKS 9

Routing in Ad-Hoc Networks- Introduction-Topology based versus Position based Approaches-Proactive, Reactive, Hybrid Routing Approach-Principles and issues – Location services - DREAM – Quorums based location service – Grid – Forwarding strategies – Greedy packet forwarding – Restricted directional flooding- Hierarchical Routing- Issues and Challenges in providing QoS.

UNIT III MAC, ROUTING & QOS IN WIRELESS SENSOR NETWORKS 9

Introduction – Architecture - Single node architecture – Sensor network design considerations – Energy Efficient Design principles for WSNs – Protocols for WSN – Physical Layer : Transceiver Design considerations – MAC Layer Protocols – IEEE 802.15.4 Zigbee – Link Layer and Error Control issues - Routing Protocols – Mobile Nodes and Mobile Robots - Data Centric & Contention Based Networking – Transport Protocols & QOS – Congestion Control issues – Application Layer support.

UNIT IV SENSOR MANAGEMENT 9

Sensor Management - Topology Control Protocols and Sensing Mode Selection Protocols - Time synchronization - Localization and positioning – Operating systems and Sensor Network programming – Sensor Network Simulators

UNIT V SECURITY IN AD HOC AND SENSOR NETWORKS 9

Security in Ad-Hoc and Sensor networks – Key Distribution and Management – Software based Anti-tamper techniques – water marking techniques – Defence against routing attacks - Secure Adhoc routing protocols – Broadcast authentication WSN protocols – TESLA – Biba – Sensor Network Security Protocols – SPINS.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Identify different issues in wireless ad hoc and sensor networks.
CO2: Understand and develop information dissemination protocols for sensor and mobile networks
CO3: Analyze protocols developed for ad hoc and sensor networks.
CO4: Identify and address the security threats in ad hoc and sensor networks.
CO5: Understand various management protocol for designing sensor nodes.
CO6: Establish a Sensor network environment for different type of applications.

REFERENCE BOOKS:

1. Carlos De Morais Cordeiro, Dharma Prakash Agrawal, Ad Hoc and Sensor Networks: Theory and Applications, Second Edition, World Scientific Publishing, 2011
2. Liehuang Zhu, Sheng Zhong, Mobile Ad Hoc and Sensor Networks, First Edition, Springer Singapore, 2018.
3. Erdal Çayırcı, Chunming Rong, Security in Wireless Ad Hoc and Sensor Networks, John Wiley and Sons, 2009.
4. Holger Karl, Andreas willing, Protocols and Architectures for Wireless Sensor

Networks, John Wiley & Sons, Inc .2007
5. Subir Kumar Sarkar, T G Basavaraju, C Puttamadappa, Ad Hoc Mobile Wireless Networks, Auerbach Publications, 2008.
6. Waltenegus Dargie, Christian Poellabauer, Fundamentals of Wireless Sensor Networks Theory and Practice, John Wiley and Sons, 2010.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE226	HIGH PERFORMANCE NETWORKS	3	0	0	3

OBJECTIVES:

- To develop a comprehensive understanding of multimedia networking
- To introduce high speed switching concepts
- To study high performance networks.
- To study the types of VPN and tunneling protocols for security
- To learn about network security in many layers and network management

UNIT I INTRODUCTION **9**

Review of OSI, TCP/IP; Multiplexing, Modes of Communication, Switching, Routing. SONET – DWDM – DSL – ISDN – BISDN, ATM.

UNIT II MULTIMEDIA NETWORKING APPLICATIONS **9**

Streaming stored Audio and Video – Best effort service – protocols for real time interactive applications – Beyond best effort – scheduling and policing mechanism – integrated services – RSVP-differentiated services.

UNIT III ADVANCED NETWORKS CONCEPTS **9**

VPN-Remote-Access VPN, site-to-site VPN, Tunnelling to PPP, Security in VPN.MPLS- operation, Routing, Tunnelling and use of FEC, Traffic Engineering, MPLS based VPN, overlay networks P2P connections.

UNIT IV TRAFFIC MODELLING **9**

Little's theorem, Need for modelling, Poisson modelling and its failure, Non- poison models, Network performance evaluation.

UNIT V NETWORK SECURITY AND MANAGEMENT **9**

Principles of cryptography – Authentication – integrity – key distribution and certification – Access control and: fire walls – attacks and counter measures – security in many layers. Infrastructure for network management – The internet standard management framework – SMI, MIB, SNMP, Security and administration – ASN.1

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Discuss advanced networks concepts

CO2: Compare and analyses the fundamental principles of various high speed communication networks and their protocol architectures

CO3: Outline traffic modeling

CO4: Evaluate network security

CO5: Compare and analyses the various routing protocols in IP networks

CO6: Describe the key components and technologies involved and to gain hands-on experiences in building state- of art network design applications.

REFERENCE BOOKS:

1. Anurag Kumar, D. M Anjunath, Joy Kuri, Communication Networking, Morgan Kaufmann Publishers, 2008.
2. Fred Halsall and Lingana Gouda Kulkarni, Computer Networking and the Internet, Fifth Edition, Pearson education 2006.
3. Hersent Gurle & Petit, IP Telephony, packet Pored Multimedia communication Systems, Pearson Education 2003
4. J.F. Kurose & K.W. Ross, Computer Networking- A top down approach featuring the internet, Pearson, Second Edition, 2003.
5. Gerry Howser, Computer Networking and the Internet: A Hands-on Approach, Springer, 2020.
6. Nader F.Mir, Computer and Communication Networks, first edition 2010.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE227	CRYPTOGRAPHY AND NETWORK SECURITY	3	0	0	3

OBJECTIVES:

- To understand the classical ciphers, and public key cryptography.
- To study block ciphers for practical implementation.
- To learn about how to maintain the Confidentiality, Integrity and Availability of a data.
- To study Hash functions and MAC functions.
- To understand and study the security issues and challenges in various networks.

UNIT I CLASSICAL CIPHERS **9**

Services – Mechanisms and Attacks – OSI security Architecture – Model for Network Security –Classical Encryption Techniques – Symmetric Cipher Model – Substitution Techniques –Transposition Techniques – Rotor Machines– Stenography

UNIT II BLOCK CIPHERS &PUBLIC KEY ENCRYPTION **9**

Block Ciphers and Data Encryption Standard – Simplified DES – Block Cipher Principles, Data Encryption Standard – Strength of DES, Block Cipher Design Principles – Block Cipher Modes of Operation. Triple DES-Blowfish-RC5 algorithm. Principles of Public Key Cryptosystems – RSA Algorithm, Key Management and other public key cryptosystems– Diffie–Hellman Key Exchange – Elliptic Curve Arithmetic – Elliptic Curve Cryptography

UNIT III HASH FUNCTIONS & MAC FUNCTIONS **9**

Message Authentication and Hash Functions – Authentication Requirements – Authentication Functions – Message Authentication Codes – Hash Functions and MACs; Hash Algorithms – MD5 Message Digest Algorithm, Secure Hash Algorithm - HMAC – Digital Signatures and

Authentication Protocols – Digital Signature Standards

UNIT IV WIRELESS NETWORK SECURITY ATTACKS 9

Security Attack issues specific to Wireless systems: Browser attack, Brute force attack - Denial of Service attack - DDoS - Worm attack - Malware attack - Web attacks - SSL attack - DNS attack - Scan attack - Other attacks –Tunneling -Gray hole and Man-in-the-middle attack. Security issues & challenges in VANETs - Ad-hoc & Sensor networks and IoT

UNIT V NETWORK ATTACKS & SECURITY PRACTICE 9

Side channel attacks- counters measures - Application of simple cryptographic algorithms in FPGA - Introduction to Quantum cryptography - and study of any two quanta based cryptographic algorithms - Web security-Secure Electronic Transaction

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Understand different types of classical and public key cryptographic algorithms
CO2: Illustrate various Public key cryptographic techniques
CO3: Remember and apply block ciphers for software and hardware applications
CO4: Evaluate the authentication algorithms
CO5: Understand various attacks existing in different networks and learn to mitigate the attacks
CO6:Summarize the intrusion detection and its solutions to overcome the attacks

REFERENCE BOOKS:

1. William Stallings, Cryptography and Network Security, Prentice Hall of India, New Delhi, Sixth Edition, 2004
2. Nichols R.K. and Lekkas P.C., Wireless Security McGraw Hill 2002
3. FatihSakiz, Sevil Sen, A survey of attacks and detection mechanisms on intelligent transportation systems: VANETs and IoV Ad Hoc Networks, 61, pp. 33–50, 2017.
4. Hagai Bar –El, Introduction to side channel attacks, Dicretix technologist limited, advanced security solutions for constrained environment.
5. http://gauss.ececs.uc.edu/Courses/c653/lectures/SideC/intro.pdf
6. Gilles Van Assche, Quantum Cryptography and Secret- Key Distillation, Cambridge University Press, 2006.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE228	MULTIMEDIA COMPRESSION TECHNIQUES	3	0	0	3

OBJECTIVES:

- To provide in-depth knowledge about text, audio, image and video compression techniques
- To introduce the concepts of multimedia communication
- To understand encoding and decoding of digital data streams.
- To introduce students to basic applications, concepts, and techniques of Data Compression.
- To understand the importance of compression technologies in today's environment

UNIT I TEXT COMPRESSION 9

Mathematical Preliminaries – Huffman coding - Arithmetic coding, Dictionary techniques – LZW family algorithms, Burrows Wheeler Transform - Move-to-front Coding – Word based compression - Dynamic Markov Compression

UNIT II AUDIO COMPRESSION 9

μ- Law and A- Law Companding – PCM, DM, DPCM, ADPCM - MPEG audio – Vocoders - Channel, Phase, CELP Vocoders, G.722, G.723 standards

UNIT III IMAGE COMPRESSION 9

Transform Coding – DCT – Wavelet based compression – EZW - SPIHT coders – JPEG - JPEG 2000 standards – JBIG, JBIG2 Standards

UNIT IV VIDEO COMPRESSION 9

Motion estimation and compensation techniques - MPEG – 1, 2, 4 and 7 – direct 3D compression - Compression based on approximation - region growing based 3D image compression - 3D Spiral JPEG

UNIT V MULTIMEDIA COMMUNICATION 9

Multimedia networking –Applications - streamed stored and audio - making the best Effort service - protocols for real time interactive Applications - Distributing multimedia - Beyond best effort service - scheduling and policing Mechanisms - Integrated services - Differentiated Services – RSVP

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Analyze various components of the multimedia systems.

CO2: Understand text, audio and 3D compression algorithms and compare their efficiencies

CO3: Apply knowledge for identifying a suitable strategy for compression of text, image, audio and video

CO4: Analyze different compression techniques and standards for image and video

CO5: Apply the compression concepts in multimedia communication.

CO6: Critically analyze different approaches of compression algorithms in multimedia related mini projects

REFERENCE BOOKS:

1. Khalid Sayeed, Introduction to Data Compression, Morgan Kauffman Harcourt India, Second Edition, 2000.
2. Jean-Luc Dugelay, Atilla Baskurt, Mohamed Daoudi, 3D Object Processing Compression, Indexing and Watermarking, Wiley 2008.
3. Mark S.Drew, Ze-Nian Li, Fundamentals of Multimedia, PHI, First Edition, 2003.
4. Yun Q.Shi, Huifang Sun, Image and Video Compression for Multimedia Engineering Fundamentals, Algorithms & Standards, and CRC press, 2003.
5. Fred Hal shall Multimedia Communication – Applications, Networks, Protocols and Standards, Pearson Education, 2007.
6. Alptekin Engin, M. and Bulent Cavusoglu, New Approach in Image Compression: 3D Spiral JPEG, IEEE Communication Letters, 2011.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE229	MEMS Based Devices	3	0	0	3

OBJECTIVES:

- To provide knowledge of semiconductors and solid mechanics to fabricate MEMS devices by understanding the essential material properties
- To study various sensing and transduction technique and educate on the rudiments of Micro fabrication techniques.
- To know about RF MEMS.
- To study about optical MEMS.
- To construct models using MEMS systems

UNIT I INTRODUCTION TO MEMS **9**

Principles of Microsystems, Nano and Microscale systems, devices, and structures, Microstructures, Axial stress and strain, Shear stress and strain, Static bending of beams and thin plates, Mechanical vibration, Stiction issue, Scaling laws in miniaturization &Materials; MEMS Materials: Substrates and Wafers, Active substrate materials, Silicon, Silicon compounds, Silicon Piezo resistors, Gallium Arsenide, Quartz, Polymers, Packaging materials.

UNIT II ACTUATION MECHANISMS IN MEMS AND FABRICATION **9**

Electrostatic Actuators: charge control, voltage control, spring suspended C, pull-in voltage, linearization methods, comb drive actuators, levitation, equivalent circuits, Piezoelectric, Thermal, Magnetic actuators, gap closers, rotary finger pull up, Electronics Interface, Feedback systems, Noise, circuit and system issues.

MEMS Fabrication: Bulk micromachining, Surface micromachining, Thin-film depositions (LPCVD, Sputtering, Evaporation), LIGA, Electroplating, Wet and dry etching, Packaging: Microsystems packaging, Interfaces in microsystem packaging, Essential packaging technologies, 3D packaging, Assembly of Microsystems, Selection of packaging materials, Current and future trends for NEMS

UNIT III RF MEMS **9**

Introduction to RF MEMS, general concepts in high frequency effects, RF MEMS Switches Introduction, Analog design and guidelines, RF switch design case studies, RF filters with MEMS Tuneable Capacitors and Inductors, RF MEMS resonators and their applications, Comparison of electrostatic and piezoelectric resonators, Case Study: Micromachined Antennas, Microstrip antenna ,Micromachining for antennas fabrication, Reconfigurable antennas, Example of RF MEMS switches and applications, design approaches

UNIT IV MOEMS **9**

Digital Micro mirror Device, Grating Light Valve, Optical switches, optical filters, arrayed waveguide grating, Electrostatic reflective light modulator, Torsion mirror (TI DMD) Micromachined optical structures, Fiber-optic couplers, Refractive lenses, Diffractive lenses, Waveguide optical systems, MEMS deformable mirrors Case study: Grating Light Valve

UNIT V MODELLING OF MEMS SYSTEMS **9**

Circuit Modelling of MEMS: resonator equivalent circuits, thermal circuits, fluidic circuits, general filter topologies, insertion loss, shape factor, resonator and couplers, circuit modelling of coupled resonators, systematic micromechanical filter design procedure, Electrostatically actuated micro-mirror, design of optical filters, case studies.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Analyze the mechanical performance of microsystems.

CO2: Understand the operational theory of common MEMS actuators and analyze different MEMS technologies.

CO3: Develop ideas in the micro machined designs for the design of reconfigurable antennas.

CO4: Analyze the engineering science and physics of MEMS devices at the micro scale in optics.

CO5: Develop new ideas and applications for MEMS devices.

CO6: Gain the technical knowledge required for computer-aided design, fabrication, analysis and characterization of nano-structured materials, micro- and nano-scale devices

REFERENCE BOOKS:

1. Gregory T.A. Kovacs, Micromachined Transducers Sourcebook, The McGraw-Hill, Inc.1998.
2. Liu, Chang, Foundations of MEMS, Second Edition, Prentice Hall, 2012.
3. Nadim Maluf, An Introduction to Micro-electromechanical Systems Engineering, Artech House, 2000.
4. Vijay Varadan, K. J. Vinoy, K. A. Jose, RF MEMS and Their applications, Wiley, 2003.
5. N.P.Mahalik, MEMS, Tata McGraw Hill, 2007.
6. Tai Ran Hsu, MEMS and Microsystems Design and Manufacture, Tata McGraw Hill,2002.

NPTEL: https://nptel.ac.in/courses/108/108/108108113/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE230	SMART ANTENNAS	3	0	0	3

OBJECTIVES:

- To study the different types of Smart Antenna System.
- To learn the benefits of smart antenna technology.
- To understand the Direction of Arrival Estimation.
- To gain an understanding and experience with smart antenna environments, algorithms and implementation.
- To study the operation of adaptive antenna array system.

UNIT I Introduction to Smart Antennas **9**

Spatial processing for wireless systems. Adaptive antennas. Beam forming networks. Digital radio receiver techniques and software radios.

UNIT II Smart Antennas Techniques for CDMA **9**

Coherent and non-coherent CDMA spatial processors. Dynamic re-sectoring. Range and capacity extension – multi-cell systems

UNIT III CDMA System Range Using Spatial Filtering **9**

Spatio–temporal channel models. Environment and signal parameters. Geometrically based

single bounce elliptical model

UNIT IV Spatial Filtering **9**

Optimal spatial filtering – adaptive algorithms for CDMA. Multitarget decision – directed algorithm.

UNIT V DOA Estimation Fundamentals **9**

DOA estimation – conventional and subspace methods. ML estimation techniques. Estimation of the number of sources using eigen decomposition. Direction finding and true ranging PL systems. Elliptic and hyperbolic PL systems. TDOA estimation techniques.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Compare the performances of digital radio receivers and software radios.
CO2: Study the CDMA spatial processors to analyze the multi-cell systems.
CO3: Analyze the channel models for smart antenna systems.
CO4: Study the environmental parameters for signal processing of smart antenna systems.
CO5: Evaluate the requirements for the design and implementation of smart antenna systems
CO6: Design practical antennas for Radar applications.

REFERENCE BOOKS:

1. T.S.Rappaport & J.C.Liberti, Smart Antennas for Wireless Communication, Prentice Hall (PTR) 1999.
2. R.Janaswamy, Radio Wave Propagation and Smart Antennas for Wireless Communication, Kluwer,2001
3. M.J. Bronzel, Smart Antennas, John Wiley, 2004
4. Constantine Balanis, Introduction to Smart Antennas, First Edition, Morgan Claypool Publishers, 2007.
5. Frank Gross, Smart Antennas for Wireless Communication, McGraw-Hill Osborne Media, 2005.
6. Gao, Steven, Gu, Chao, Liu, Wei, Luo, Qi, Low Cost Smart Antennas, First Edition, John Wiley & Sons, 2019.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE231	RF IC DESIGN	3	0	0	3

OBJECTIVES:

- To study basics of RF IC design and the architectures of RF transceivers
- To understand the concepts of design and analysis of modern RF and wireless communication integrated circuits
- To familiarize with the circuit level design of building blocks of RF transceivers
- To understand the principles, analysis, and design of Low-Noise-Amplifier (LNA), mixer,

Voltage-Controlled-Oscillator (VCO), and Phase-Locked-Loop (PLL).

- To carry out performance analysis of RF transceivers

UNIT I RF IC DESIGN BACKGROUND 9

Introduction to RF Circuit Design - Basic Concepts in RF Design: General Considerations, Effects of Nonlinearity, Noise, Sensitivity and Dynamic Range, Passive Impedance Transformation, Scattering Parameters, Analysis of Nonlinear Dynamic Systems, Volterra Series

Transceiver Architectures: General Considerations, Receiver Architectures, Transmitter Architectures

UNIT II IMPEDANCE MATCHING & LOW-NOISE AMPLIFIERS 9

Impedance Matching: Definition of Q, Impedance Matching using L, PI and T networks, Integrated Inductors, Resistors, Capacitors, Tuneable inductors, Transformers

Low-Noise Amplifiers: General Considerations, Problem of Input Matching, LNA Topologies, Gain Switching, Band Switching, High-IP2 LNAs, Nonlinearity Calculations

UNIT III MIXERS & OSCILLATORS 9

Mixers: General Considerations, Passive Down-conversion Mixers, Active Down conversion Mixers, Improved Mixer Topologies, Up-conversion Mixers

Oscillators: Performance Parameters, Basic Principles, Cross-Coupled Oscillator, Three-Point Oscillators, Voltage-Controlled Oscillators, LC VCOs with Wide Tuning Range, Phase Noise, Design Procedure - Low-Noise VCOs, LO Interface, Mathematical Model of VCOs, Quadrature Oscillators.

UNIT IV PHASE-LOCKED LOOPS & FREQUENCY SYNTHESIZERS 9

Phase-Locked Loops: Basic Concepts, Type-I PLLs, Type-II PLLs, PFD/CP Nonidealities, Phase Noise in PLLs, Loop Bandwidth, Design Procedure

Integer-N Frequency Synthesizers: General Considerations, Basic Integer-N Synthesizer, Settling Behaviour, Spur Reduction Techniques, PLL-Based Modulation, Divider Design

Fractional-N Synthesizers: Basic Concepts, Randomization and Noise Shaping, Quantization Noise Reduction Techniques

UNIT V POWER AMPLIFIERS & TRANSCEIVER DESIGN 9

Power Amplifiers: General Considerations, Classification of Power Amplifiers, High-Efficiency Power Amplifiers, Cascade Output Stages, Large-Signal Impedance Matching, Basic Linearization Techniques, Polar Modulation, Out phasing, Doherty Power Amplifier, Design Examples

CMOS Transceiver Design: System-Level Considerations, Receiver Design, Transmitter Design, Synthesizer Design

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Understand the fundamentals of RF IC design.
CO2: Design circuit level design of building blocks of RF transceivers using CMOS technology.
CO3: Design monolithic inductors for integrated amplifiers and oscillators.
CO4: Discuss monolithic synthesizer architectures and their performance.
CO5: Analyze various performance parameters of RF transceivers.
CO6: Derive the Class A, AB, B, C amplifiers, Class D, E, F amplifiers, RF Power amplifier design and to perform simple projects.

REFERENCE BOOKS:

1. Razavi B, RF Microelectronics, Pearson Education, Second Edition, 2012.
2. Thomas H.Lee, The Design of CMOS Radio –Frequency Integrated Circuits, Cambridge University Press, Second Edition, 2004.
3. Bosco H Leung VLSI for Wireless Communication, Pearson Education, Second Edition, 2011.
4. Behzad Razavi, Design of CMOS Analog Integrated Circuits, McGraw Hill Publications, Second Edition, 2017.
5. Hooman Darabi, Radio Frequency Integrated Circuits and Systems, Cambridge University Press, First Edition, 2015.
6. Cam Nguyen, Radio Frequency Integrated Circuit Engineering, First Edition, John Wiley & Sons, 2015.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE232	MICROWAVE INTEGRATED CIRCUITS	3	0	0	3

OBJECTIVES:

- To have the essential knowledge of various planar microstrip circuits.
- To design and analyses various types of microwave planar circuits.
- To understand the concept of non-reciprocal components, active devices, High Power and Low Power Circuits.
- To provide basic information on microstrip resonators.
- To acquaint the fabrication techniques and tolerances for MIC circuits

UNIT I Planar Transmissions Lines **9**

Introduction, types of MICs and their technology, types of planar transmission lines, introduction to coupled micro strip lines, slot lines and co-planar waveguides, Fields of propagation in micro strip lines, design equations of micro strip lines (characteristic impedance and W/H relation)

UNIT II Lumped elements for MICs **9**

Losses in micro strip lines, discontinuities in micro strip lines, Lumped micro strip components: Design of micro strip and chip inductors, capacitors, resistors. Quasi lumped micro strip elements: Open and short-circuited stubs (quarter wavelength, half wavelength)

UNIT III Microstrip Resonators **9**

Microwave resonators: Quarter & Half wave length resonators, Ring resonators: types, advantages and applications, Patch resonators. Even and Odd mode analysis of equal &unequal Wilkinson Power Divider, Even & Odd mode analysis of branch line coupler and 180^{o} hybrid coupler.

UNIT IV Band pass Filter Design **9**

Coupled line coupler and its S-matrix, Ring coupler and its S-matrix, Band Pass Filter: Insertion loss method, Conversion from low pass to band pass, Design of band pass filter using lumped elements, distributed elements, impedance inverters, and coupled lines.

UNIT V MIC & MMIC Fabrication Technologies **9**

Hybrid MICs, Configuration, Dielectric substances, thick and thin film technology, LTCC, HTCC,

Printed Circuit Board technology (PCB), Fabrication process of MMIC.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Comprehend the importance of various micro strip lines and the losses due to various micro strip discontinuities.

CO2: Understand the design of lumped elements for microwave circuits.

CO3: Design and analyze various micro strip resonators.

CO4: Design and analyze microstrip power dividers, couplers and band pass filters.

CO5: Appreciate and evaluate the performance of various fabrication techniques for planar circuits

CO6: Evaluate the performance of microwave integrated circuits by using different measurements and testing techniques.

REFERENCE BOOKS:

1. D. M. Pozar, Microwave engineering, fourth Edition, John Wiley, India, 2012.
2. Gonzalez, Guillermo, Microwave transistor amplifiers: analysis and design, Prentice hall, 1997.
3. Leo G. Maloratsky, RF & Microwave Integrated Circuits: Passive components and control devices, First Edition, Elsevier Inc., India 2012.
4. Andrei Grebennikov, RF and Microwave Transistor Oscillator Design, First Edition, Wiley, 2007.
5. S. Raghavan, Microwave Integrated Circuit Components Design through MATLAB, CRC Press, 2020.
6. Stephen A. Maas, Non Linear Microwave and RF Circuits, Artech House, Second Edition, 2003.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE321	Pattern Recognition and Machine learning	3	0	0	3

OBJECTIVES:

- To introduce the fundamentals of pattern recognition techniques
- To understand various clustering techniques
- To introduce sequential pattern recognition methods
- To introduce the concepts of support vector machines
- To introduce the fundamentals of neural networks

UNIT I PATTERN CLASSIFICATION 9

Overview of pattern recognition, Supervised learning. Bayes decision theory, Minimum-error-rate classification, Classifiers, Discriminant functions, and Decision surfaces. Normal density (univariate and multivariate) and discriminant functions for the normal density. Discrete features. Parameter estimation methods: Maximum likelihood estimation, Maximum a posteriori estimation. Bayesian estimation: Gaussian case. Pattern classification by distance functions - minimum distance classifier.

UNIT II CLUSTERING 9

Unsupervised learning and clustering - criterion functions for clustering. Algorithms for clustering - k-means and hierarchical clustering, Cluster validation. Expectation-maximization algorithm. Gaussian mixture models, model selection for latent variable models, high-dimensional spaces, the curse of dimensionality, dimensionality reduction, factor analysis, Principal component analysis, probabilistic PCA, Independent component analysis.

UNIT III PROBABILISTIC GRAPHICAL MODELS 9

Directed graphical models - Bayesian network. From distributions to graphs - examples-Markov Random fields-inference in graphical models - Markov model - Hidden Markov Models (HMMs) - building a hidden Markov model for multi-class pattern recognition, issues.

UNIT IV SUPPORT VECTOR MACHINES 9

Constrained optimization problems - linearly separable and non-separable patterns, hyperplane and margin - discriminant function of a hyperplane, maximum margin hyperplane. Kernel functions -vector kernels - linear, polynomial and Gaussian kernels, non-vector kernels. Building a support-vector machine for multi-class pattern recognition - architecture, choice of kernels, issues.

UNIT V ARTIFICIAL NEURAL NETWORKS 9

Models of a neuron - feed-forward neural networks - Perceptron learning, Multi-layer feed-forward neural network, Gradient descent, back propagation algorithm - network pruning, limitations and convergence of back-propagation learning. Cover's theorem on the separability of patterns, Generalized radial-basis function networks, Auto encoder networks - auto-association neural network - convolutional neural network.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Classify the data and identify the patterns

CO2: Apply dimensionality reduction techniques

CO3: Choose an appropriate pattern recognition system for the given data

CO4: Solve linearly non-separable pattern recognition problems using SVMs

CO5: Apply neural networks for suitable pattern recognition problems

CO6: Apply Auto encoder and convolutional neural networks for pattern recognition problems.

REFERENCE BOOKS:

1. Duda R.O, Hart P.E. and Stork D.G, Pattern Classification, John Wiley, 2001.
2. Bishop C.M, Pattern Recognition and Machine Learning, Springer, First Edition,2006.
3. Theodoridis S and Koutroumbas K, Pattern Recognition, Academic Press, Fourth Edition, 2009.
4. Simon Haykin, Neural networks - a comprehensive foundation, Pearson Education, Second Edition, 2008.
5. Goodfellow Y. Bengio and A. Courville, Deep Learning, MIT Press, First Edition, 2016.
6. Joao Luis G. Rosa, Artificial Neural Networks - Models and Applications, IN-TECH, 2016.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE322	DATA CONVERTERS	3	0	0	3

OBJECTIVES:

- To understand the Basic operational and design principles of CMOS ADC and DAC architectures.
- To understand signal sampling and conversion of information from analog to digital domains
- To introduce Design estimation techniques for developing various functional blocks associated with both the ADC and DAC architectures.

- Learn to design switched-capacitor circuits.
- To introduce bias considerations for all the functional models as part of data converters.

UNIT I SAMPLE AND HOLD CIRCUITS 9

Sampling switches - Conventional open loop and closed loop sample and hold architecture - Open loop architecture with miller compensation - Multiplexed input architectures - Recycling architecture switched capacitor architecture - Performance metrics of ADC and DAC - Issues in sampling, quantization and reconstruction, oversampling and anti-aliasing filters

UNIT II SWITCHED CAPACITOR CIRCUITS AND COMPARATORS 9

Switched capacitor amplifiers - Switched capacitor integrator - Switched capacitor common mode feedback - Single stage amplifier as comparator - Cascaded amplifier stages as comparator Latched comparators - Offset cancellation, Op Amp offset cancellation and Calibration techniques

UNIT III NYQUIST RATE DIGITAL TO ANALOG CONVERSION 9

Reference multiplication and division - Resistor ladder DAC architecture - Current Steering DACs - Switching and logic functions in DAC - Capacitive DACs, Binary weighted versus thermometer DACs - Issues in current element matching - Clock feed through, zero order hold circuits - Differential nonlinearity - Integral non-linearity

UNIT IV ANALOG TO DIGITAL CONVERSION 9

Flash ADC: Reference ladder DC and AC bowing - Non-linear input capacitance, kickback noise, slew-dependent sampling point - Pipelined ADC: two-step ADC - Successive approximation architecture (SAR) ADC: charge redistribution architecture in DAC - Time interleaved ADC - Range overlap and digital correction.

UNIT V SIGMA DELTA CONVERTERS 9

Fist order and second order Delta Sigma Modulators (DSM) - Signal Dependent Stability of DSMs - Maximum Stable Amplitude of DSMs - Systematic NTF Design - Computation of in-band SNR - Continuous-time Delta Sigma Modulators (CTDSM) - Inherent anti-aliasing property of CTDSMs - Effect of op amp non-ideologies - Finite gain bandwidth - Effect of ADC and DAC non-ideologies

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Create and analyze sample and hold circuits.
CO2: Understand the concepts of switched capacitors circuits and comparators
CO3: Create and analyze analog to digital and digital to analog converters.
CO4: Analyze ADC and DAC architectures and its performance.
CO5: Understand calibration techniques.
CO6: Explain Sigma Delta Converters.

REFERENCE BOOKS:

1. Behzad Razavi, Principles of data conversion system design, IEEE Press, 1995.
2. Franco Maloberti, Data Converters, Springer, 2007.
3. Rudy V and Plassche, CMOS integrated Analog-to-digital and Digital-to-Analog converters, Kluwer Academic Publishers, 2003.
4. Shanthi Pavan, Richard Schreier and Gabor C. Temes, Understanding Delta-Sigma Data Converters, IEEE Press, Wiley, Second Edition, 2017.

5. Analog Devices Inc., edited by Walt Kester, The Data Conversion Handbook, Newness Elsevier, 2005.
6. David A. Johns, Kenneth W. Martin, Analog Integrated Circuit Design, Second Edition, John Wiley & Sons 2012.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE323	SOLID STATE DEVICE MODELLING AND SIMULATION	3	0	0	3

OBJECTIVES:

- To understand the concept of device modeling.
- To adequate understanding of semiconductor device modeling aspects, useful for designing devices in electronic, and optoelectronic applications.
- To understand the concept of noise modeling.
- To learn multistep method.
- To study device simulations.

UNIT I MOSFET DEVICE PHYSICS 9

Capacitor, Basic operation, Basic modeling, Advanced MOSFET modelling, RF modeling of MOS transistors, Equivalent circuit representation of MOS transistor, High frequency behavior of MOS transistor and AC small signal modeling, Model parameter extraction, Modeling parasitic BJT, Resistors, Capacitors, Inductors.

UNIT II NOISE MODELLING 9

Noise sources in MOSFET, Flicker noise modeling, Thermal noise modeling, Model for accurate distortion analysis, Non-linearities in CMOS devices and modeling, Calculation of distortion in analog CMOS circuits.

UNIT III DEVICE MODELING 9

Prime importance of circuit and device simulations in VLSI: Nodal, Mesh, Modified nodal and Hybrid analysis equations, Solution of network equations: Sparse matrix techniques, Solution of nonlinear networks through Newton-Raphson technique, Convergence and stability.

UNIT IV MATHEMATICAL TECHNIQUES DEVICE SIMULATIONS 9

Poisson equation, continuity equation, drift-diffusion equation, Schrodinger equation, Hydrodynamic equations, Trap rate, Finite difference solutions to these equations in 1D and 2D space, grid generation.

UNIT V SIMULATION OF DEVICES 9

Computation of characteristics of simple devices like p-n junction, MOS capacitor and MOSFET; Small-signal analysis

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Explain the importance of MOS Capacitor and Small signal modeling
CO2: Apply and determine the drift diffusion equation and stiff system equation.
CO3: Analyze circuits using parasitic BJT parameters and newton Raphson method.
CO4: Model the MOS transistor using Schrodinger equation and Multistep methods.
CO5: Analyze the small signal MOSFET using model

CO6: Calculate the threshold voltages for different MOSFETS and compute the junction capacitances

REFERENCE BOOKS:

1. Arora, N., MOSFET Modelling for VLSI Simulation, Cadence Design Systems, 2007.
2. Chua, L.O. and Lin, P.M., Computer-Aided Analysis of Electronic Circuits: Algorithms and Computational Techniques, Prentice-Hall., 1975.
3. Fjeldly, T., Yetterdal, T. and Shur, M., Introduction to Device Modeling and Circuit Simulation, Wiley-Interscience., 1997.
4. Grasser, T., Advanced Device Modeling and Simulation, World Scientific Publishing Company. 2003.
5. Selberherr, S., Analysis and Simulation of Semiconductor Devices, Second Edition, Springer-Verlag., 2011.
6. Tsividis, Y., Operation and Modelling of the MOS Transistor, Second Edition, Oxford University Press, 2010.

WEB URLs:

1. http://www.asc.tuwien.ac.at/~juengel/scripts/semicond.pdf
2. http://www.iacs.res.in/ijp/ijp_january_06_rev.pdf

COURSE CODE	COURSE TITLE	L	T	P	C
20AE324	SPEECH AND AUDIO SIGNAL PROCESSING	3	0	0	3

OBJECTIVES:

- To study basic concepts of processing speech and audio signals.
- To study and analyses various M-band filter-banks for audio coding.
- To understand audio coding based on transform coders.
- To understand speech synthesis and speech recognition.
- To study time and frequency domain speech processing methods.

UNIT I MECHANICS OF SPEECH AND AUDIO 9

Introduction - Review of Signal Processing Theory-Speech production mechanism – Nature of Speech signal – Discrete time modelling of Speech production – Classification of Speech sounds – Phones – Phonemes – Phonetic and Phonemic alphabets – Articulatory features. Absolute Threshold of Hearing - Critical Bands- Simultaneous Masking, Masking-Asymmetry, and the Spread of Masking- Non-simultaneous Masking - Perceptual Entropy - Basic measuring philosophy -Subjective versus objective perceptual testing - The perceptual audio quality measure (PAQM) - Cognitive effects in judging audio quality.

UNIT II TIME-FREQUENCY ANALYSIS: FILTER BANKS AND TRANSFORMS 9

Introduction - Analysis-Synthesis Framework for M-band Filter Banks- Filter Banks for Audio Coding: Design Considerations - Quadrature Mirror and Conjugate Quadrature Filters - Tree-Structured QMF and CQF M-band Banks - Cosine Modulated “Pseudo QMF” M-band Banks -Cosine Modulated Perfect Reconstruction (PR) M-band Banks and the Modified Discrete Cosine Transform (MDCT) - Discrete Fourier and Discrete Cosine Transform - Pre-echo Distortion- Pre-echo Control Strategies.

UNIT III AUDIO CODING AND TRANSFORM CODERS **9**

Lossless Audio Coding – Lossy Audio Coding - ISO-MPEG-1A, 2A, 2A-Advaned, 4A Audio Coding - Optimum Coding in the Frequency Domain - Perceptual Transform Coder –Brandenburg - Johnston Hybrid Coder - CNET Coders - Adaptive Spectral Entropy Coding –Differential Perceptual Audio Coder - DFT Noise Substitution -DCT with Vector Quantization -MDCT with Vector Quantization.

UNIT IV MATHEMATICAL TECHNIQUES DEVICE SIMULATIONS **9**

Time domain parameters of Speech signal – Methods for extracting the parameters: Energy, Average Magnitude – Zero crossing Rate – Silence Discrimination using ZCR and energy Short Time Fourier analysis – Formant extraction – Pitch Extraction using time and frequency domain methods Homomorphic Speech Analysis: Cepstral analysis of Speech – Formant and Pitch Estimation – Homomorphic Vocoders.

UNIT V PREDICTIVE ANALYSIS OF SPEECH **9**

Formulation of Linear Prediction problem in Time Domain – Basic Principle – Auto correlation method – Covariance method – Solution of LPC equations – Cholesky method – Durbin's Recursive algorithm – lattice formation and solutions – Comparison of different methods – Application of LPC parameters – Pitch detection using LPC parameters – Formant analysis – VELP – CELP-RELP.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Evaluate audio coding and transform coders

CO2: Discuss time and frequency domain methods for speech processing

CO3: Explain predictive analysis of speech

CO4: Explain the main principles of common audio signal processing operations

CO5: Design and implement algorithms for processing audio and speech signals using MATLAB.

CO6: Compare the different methods of Linear Prediction like VELP, CELP and RELP.

REFERENCE BOOKS:

1. B.Gold and N.Morgan, Speech and Audio Signal Processing, Wiley and Sons, 2000.
2. L.R.Rabiner and R.W.Schaffer, Digital Processing of Speech Signals, Pearson Education India, 2003.
3. Mark Kahrs, Karlheinz Brandenburg, Kluwer Applications of Digital Signal Processing to Audio and Acoustics, Auris Reference, 2017.
4. Udo Zolzer, Digital Audio Signal Processing, Second Edition A John Wiley& sons, 2008.
5. Vijay K. Madisetti, The Digital Signal Processing Handbook: Video, Speech and Audio Signal Processing, CRC Press, 2009.
6. Paul Hill, Audio and Speech Processing with MATLAB, First Edition, CRC Press, 2020.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE325	PHYSICAL DESIGN OF VLSI CIRCUITS	3	0	0	3

OBJECTIVES:

- To study various physical design methods in VLSI.
- To understand the concepts behind the VLSI design rules and routing techniques
- To introduce the physical design concepts such as placement, partitioning and packaging

- To learn various floor planning methods for system design.
- To study the performance of circuits layout designs, compaction techniques

UNIT I INTRODUCTION TO VLSI TECHNOLOGY 9

Layout Rules-Circuit abstraction Cell generation using programmable logic array transistor chaining, Wein Berger arrays and gate matrices-layout of standard cells gate arrays and sea of gates, field programmable gate array(FPGA)-layout methodologies Packaging-Computational Complexity - Algorithmic Paradigms.

UNIT II PLACEMENT USING TOP-DOWN APPROACH 9

Partitioning: Approximation of Hyper Graphs with Graphs, Kernighan-Lin Heuristic Ratio cut partition with capacity and i/o constraints. Floor planning: Rectangular dual floor planning hierarchical approach- simulated annealing- Floor plan sizing Placement: Cost function- force directed method-placement by simulated annealing partitioning placement- module placement on a resistive network – regular placement linear placement.

UNIT III ROUTING USING TOP DOWN APPROACH 9

Fundamentals: Maze Running- line searching- Steiner trees Global Routing: Sequential Approaches - hierarchical approaches - multi commodity flow-based techniques - Randomised Routing- One Step approach - Integer Linear Programming Detailed Routing: Channel Routing - Switch box routing. Routing in FPGA: Array based FPGA- Row based FPGAs

UNIT IV PERFORMANCE ISSUES IN CIRCUIT LAYOUT 9

Delay Models: Gate Delay Models- Models for interconnected Delay- Delay in RC trees. Timing – Driven Placement: Zero Stack Algorithm- Weight based placement- Linear Programming Approach Timing Riving Routing: Delay Minimization- Click Skew Problem- Buffered Clock Trees. Minimization: constrained via Minimization unconstrained via Minimization- Other issues in minimization

UNIT V SINGLE LAYER ROUTING, CELL GENERATION AND COMPACTION 9

Planar subset problem(PSP)- Single Layer Global Routing- Single Layer detailed Routing- Wire length and bend minimization technique –Over The Cell (OTC) Routing Multiple chip modules(MCM)-programmable Logic Arrays- Transistor chaining- Wein Burger Arrays- Gate matrix layout- 1D compaction- 2D compaction.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1:Explain different types of routing

CO2: Understand the concepts of Physical Design Process such as partitioning, Floor planning, and Placement.

CO3: Outline 1D compaction- 2D compaction

CO4: Discuss the various performance issues in circuit layout

CO5: Discuss the concepts of design optimization algorithms and their application to physical design automation.

CO6: Explain the different logic arrays.

REFERENCE BOOKS:

1. Preas M. Lorenzatti, Physical Design and Automation of VLSI systems, The Benjamin Cummins Publishers, 1998.
2. Sarafzadeh, C.K. Wong, An Introduction to VLSI Physical Design, McGraw Hill Int.

Edition 1995.

3. Wayne Wolf, Modern VLSI Design – System – on – Chip Design, Third Edition, Prentice Hall, 2008.
4. Wayne Wolf, Modern VLSI Design – IP based Design, Fourth Edition, Prentice Hall, 2008.
5. N.A. Sherwani, Algorithms for VLSI Physical Design Automation, Springer International Edition Third Edition, 2005.
6. Veena S. Chakravarthi, A Practical Approach to VLSI System on Chip Design, Springer, 2019.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE326	ROBOTICS AND INTELLIGENT SYSTEMS	3	0	0	3

OBJECTIVES:

- To teach the basic concepts in robotics.
- To expose the various design aspects in robot grippers.
- To make learn various drives and control systems.
- To impart knowledge on machine vision systems.
- To apply robot-based concepts for automation

UNIT I INTRODUCTION **9**

Basic Concepts such as Definition, three laws, DOF, Misunderstood devices etc., Elements of Robotic Systems i.e. Robot anatomy, Classification, Associated parameters i.e. resolution, accuracy, repeatability, dexterity, compliance, RCC device, etc. Automation-Concept, Need, Automation in Production System, Principles and Strategies of Automation, Basic Elements of an Automated System, Advanced Automation Functions, Levels of Automations, introduction to automation productivity.

UNIT II ROBOT GRIPPERS **9**

Types of Grippers, Design aspect for gripper, Force analysis for various basic gripper system. Sensors for Robots: - Characteristics of sensing devices, Selections of sensors, Classification and applications of sensors. Types of Sensors, Need for sensors and vision system in the working and control of a robot.

UNIT III DRIVES AND CONTROL SYSTEMS **9**

Types of Drives, Actuators and its selection while designing a robot system. Types of transmission systems, Control Systems -Types of Controllers, Introduction to closed loop control. Control Technologies in Automation: - Industrial Control Systems, Process Industries Verses Discrete-Manufacturing Industries, Continuous Verses Discrete Control, Computer Process and its Forms. Control System Components such as Sensors, Actuators and others.

UNIT IV MACHINE VISION SYSTEM **9**

Vision System Devices, Robot Programming: - Methods of robot programming, lead through programming, motion interpolation, branching capabilities, WAIT, SIGNAL and DELAY commands, subroutines, Programming Languages: Introduction to various types such as RAIL and VAL II etc, Features of type and development of languages for recent robot systems.

UNIT V MODELLING AND SIMULATION FOR MANUFACTURING PLANT AUTOMATION **9**

Introduction, need for system Modelling, Building Mathematical Model of a manufacturing Plant, Modern Tools- Artificial neural networks in manufacturing automation, AI in manufacturing, Fuzzy

decision and control, robots and application of robots for automation. Artificial Intelligence: - Introduction to Artificial Intelligence, AI techniques, Need and application of AI. Other Topics in Robotics: - Socio-Economic aspect of robotisation. Economical aspects for robot design, Safety for robot and associated mass, New Trends & recent updates in robotics.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Implement simple concepts associated with Robotics and Automation

CO2: Use various Robotic sub-systems

CO3: Use kinematics and dynamics to design exact working pattern of robots

CO4: Implement computer vision algorithms for robots

CO5: Be aware of the associated recent updates in Robotics

CO6: Illustrate the applications of AI in Robotic Applications

REFERENCE BOOKS:

1. John J. Craig, Introduction to Robotics (Mechanics and Control), Addison-Pearson, Fourth Edition, 2017.
2. Mikell P. Groover et. al., Industrial Robotics: Technology, Programming and Applications, McGraw – Hill International, Second Edition, 2017.
3. Sanfeliu A., Handbook of Industrial Robotics Technology and Applications, Auris Reference, 2016.
4. Mikell. P. Groover, Automation, Production Systems and Computer Integrated Manufacturing, M.P. Groover, Pearson Education, 2016.
5. Chanchal Dey, Sunit Kumar Sen, Industrial Automation Technologies, CRC Press, First Edition, 2020.
6. Richard D. Klafter, Thomas A. Chmielewski, Michael Negin, Robotic Engineering: An Integrated Approach , Prentice Hall India, 2010.

NPTEL:https://nptel.ac.in/courses/107/106/107106090/

COURSE CODE	COURSE TITLE	L	T	P	C
20AE327	SYSTEM ON CHIP DESIGN	3	0	0	3

OBJECTIVES:

- To understanding of issues and tools related to ASIC/FPGA design.
- To understanding of basics of System on Chip and Platform based design.
- To Understanding of the concepts, issues, and process of designing highly integrated SoCs
- To study about systematic hardware/software co-design & co-verification principles
- To prepare the student to be an entry-level industrial standard ASIC or FPGA designer.

UNIT I INTRODUCTION **9**

Introduction to SOC Design, system level design, methodologies and tools, system hardware: IO, communication, processing units, memories; operating systems: prediction of execution, Real time scheduling, embedded OS, middle ware; Platform based SOC design,

multiprocessor SOC and Network on Chip, Low power SOC Design.

UNIT II SYSTEM LEVEL MODELLING 9

System C: overview, Data types, modules, notion of time, dynamic process, basic channels, structure communication, ports and interfaces, Design with examples

UNIT III HARDWARE SOFTWARE CO-DESIGN 9

Analysis, partitioning, high level optimisations, real-time scheduling, hardware acceleration, voltage scaling and power management; Virtual platform models, co-simulation and FPGAs for prototyping of HW/SW systems

UNIT IV SYNTHESIS 9

System synthesis: Transaction Level Modelling (TLM) based design, automatic TLM generation and mapping, platform synthesis; software synthesis: code generation, multi task synthesis, internal and external communication; Hardware synthesis: RTL architecture, Input models, estimation and optimisation, resource sharing and pipelining and scheduling

UNIT V SOC VERIFICATION AND TESTING 9

SoC and IP integration, Verification: Verification technology options, verification methodology, overview: system level verification, physical verification, hardware/software co-verification; Test requirements and methodologies, SoC design for testability - System modelling, test power dissipation, test access mechanism

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Analyze algorithms and architecture of hardware software in order to optimize the system based on requirements and implementation constraints

CO2: Model and specify systems at high level of abstraction

CO3: Appreciate the co-design approach and virtual platform models

CO4: Understand hardware, software and interface synthesis

CO5: Explain the concept of system on chip (SoC) through standard design methodology and appropriate software packages.

CO6: Acquire knowledge about Front-end and back-end chip design.

REFERENCE BOOKS:

1. D. Gajski, S. Abdi, A. Gerstlauer, G. Schirner, Embedded System Design: Modeling, Synthesis, Verification, Springer, 2009.
2. Erik Larson, Introduction to advanced system-on-chip test design and optimization, Springer 2005.
3. Ghenassia, F. Transaction-level modeling with System C: TLM concepts and applications for embedded systems, Springer, 2010.
4. Hoi-junyoo, Kangmin Lee, Jun Kyoungkim, Low power NoC for high performance SoC design, CRC press, 2008.
5. M. L. Bushnell and V.D. Agrawal, Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits, Springer, 2005.
6. Vijay K. Madisetti Chonlameth Arpikanondt, A Platform-Centric Approach to System-on-Chip (SOC) Design, Springer, 2005.

COURSE CODE	COURSE TITLE	L	T	P	C
20AE328	FOUNDATIONS OF ARTIFICIAL INTELLIGENCE AND DATA SCIENCE	3	0	0	3

OBJECTIVES:

- To produce "intelligent" systems, Knowledge representation (both symbolic and neural network), search and machine learning
- To learn the principles and fundamentals of designing AI programs
- To apply different techniques in applications which involve perception, reasoning and learning
- To provide a basic exposition to the goals and methods of Artificial Intelligence.
- To understand the fundamental concepts and techniques for approaching artificial intelligence and data science

UNIT I INTRODUCTION TO ARTIFICIAL INTELLIGENCE AND DATA SCIENCE **9**

Concept of AI, history, current status, scope, agents, environments, Problem Formulations, Review of tree and graph structures, State space representation, Search graph and Search tree. Concept of Data Science, Traits of Big data, Web Scraping, Analysis vs Reporting

UNIT II SEARCH ALGORITHMS **9**

Random search, Search with closed and open list, Depth first and Breadth first search, Heuristic search, Best first search, A* algorithm, Game Search

UNIT III PROBABILISTIC REASONING **9**

Probability, conditional probability, Bayes Rule, Bayesian Networks- representation, construction and inference, temporal model, hidden Markov model.

UNIT IV PROGRAMMING TOOLS FOR DATA SCIENCE **9**

Toolkits using Python: Matplotlib, NumPy, Scikit-learn, NLTK, Visualizing Data: Bar Charts, Line Charts, Scatterplots, working with data: Reading Files, Scraping the Web, Using APIs (Example: Using the Twitter APIs), Cleaning and Munging, Manipulating Data, Rescaling, Dimensionality Reduction

UNIT V MACHINE LEARNING **9**

Overview of Machine learning concepts – Over fitting and train/test splits, Types of Machine learning – Supervised, Unsupervised, Reinforced learning, Introduction to Bayes Theorem, Linear Regression-model assumptions, regularization (lasso, ridge, elastic net), Classification and Regression algorithms-Naïve Bayes, K-Nearest Neighbors, logistic regression, support vector machines (SVM), decision trees, and random forest, Classification Errors, Analysis of Time Series- Linear Systems Analysis, Overview of Deep Learning.

TOTAL PERIODS: 45

OUTCOMES:

On successful completion of this course, the student will be able to

CO1: Learn the concepts of artificial intelligence and data science

CO2: Study problem solving techniques

CO3: Understand the representation of knowledge and reasoning mechanism

CO4: Collect explore, clean, munge and manipulate data.

CO5: Implement models such as k-nearest Neighbours, Naive Bayes, linear and logistic regression, decision trees, neural networks and clustering.

CO6: Build data science applications using Python based toolkits

REFERENCE BOOKS:

1. Stuart Russell and Peter Norvig, Artificial Intelligence: A Modern Approach, 3rd Edition, PHI 2009.
2. Elaine Rich and Kevin Knight, “Artificial Intelligence”, Tata McGraw Hill, 2010.
3. Nils J Nilsson, Principles of Artificial Intelligence, Illustrated Reprint Edition, Springer Heidelberg, 2014.
4. Saroj Kaushik, Artificial Intelligence, Cengage Learning India, 2011.
5. Trivedi.M.C. A Classical Approach to Artificial Intelligence, Khanna Publishing House, Delhi, 2018.
6. Aurélien Géron, "Hands-On Machine Learning with Scikit-Learn and Tensor Flow: Concepts, Tools, and Techniques to Build Intelligent Systems", Second Edition, O'Reilly Media, 2019.

NPTEL: https://nptel.ac.in/courses/112/103/112103280/